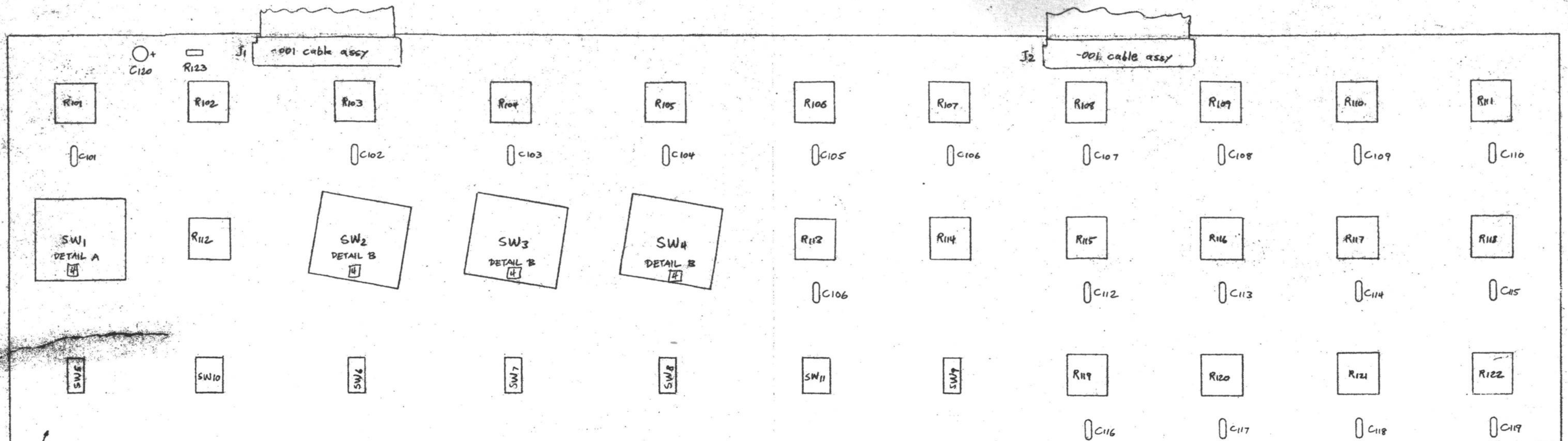
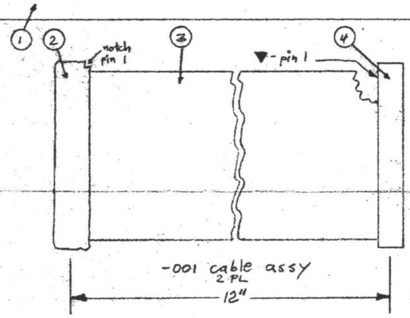




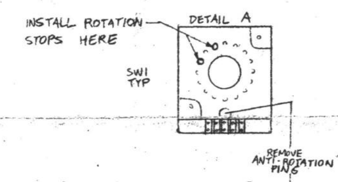
NOTES:

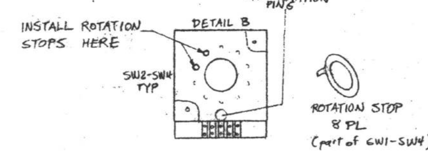
[1] FORM LEADS WITH JIG #10043 PRIOR TO INSERTION.

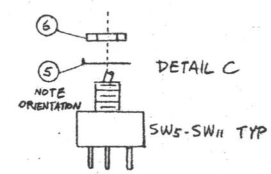
[2] deleted

[3] TOGGLE SWITCHES ARE INSTALLED WITH NOTCH ON BUSHING IN 12 O'CLOCK POS. ADD ITEMS 5 & 6 PRIOR TO NEXT ASSEMBLY (33741) SEE DETAIL C

[4] INSTALL ROTATION STOPS PER DETAILS A AND B







		ID	DESC	VAL	MFG	CODE
3 66	3	R101-R122	100K LIN POTENTIOMETER [1]	91A1D-B24-B20	BOURNS	(22)
2	2	R123	10 1/4W 5%	SBB1/4-10 Ω 5%	DALE	(1)
36	2	C101-C119	0.1µF 50V (C111 deleted)	RPE112 Z5U 104M	MURATA	(18)
2	2	C120	10µF 25V TANT	TAPS10M25	ITT	(1)
5	5	SW1	COMP. HEX ROTARY (STOCK #25987-1)	80-4530-58-1	AMP	(1)
15	5	SW2-SW4	COMP. BCD ROTARY (STOCK #36022-1)	80-4530-59-1	AMP	(3)
18	3	SW5-SW9	ON-ON SPDT [3]	7101LIPYCBE	C&K	(5)
12	6	SW10, SW11	ON-ON-ON DPDT [3]	7111LIPYCBE	C&K	(2)

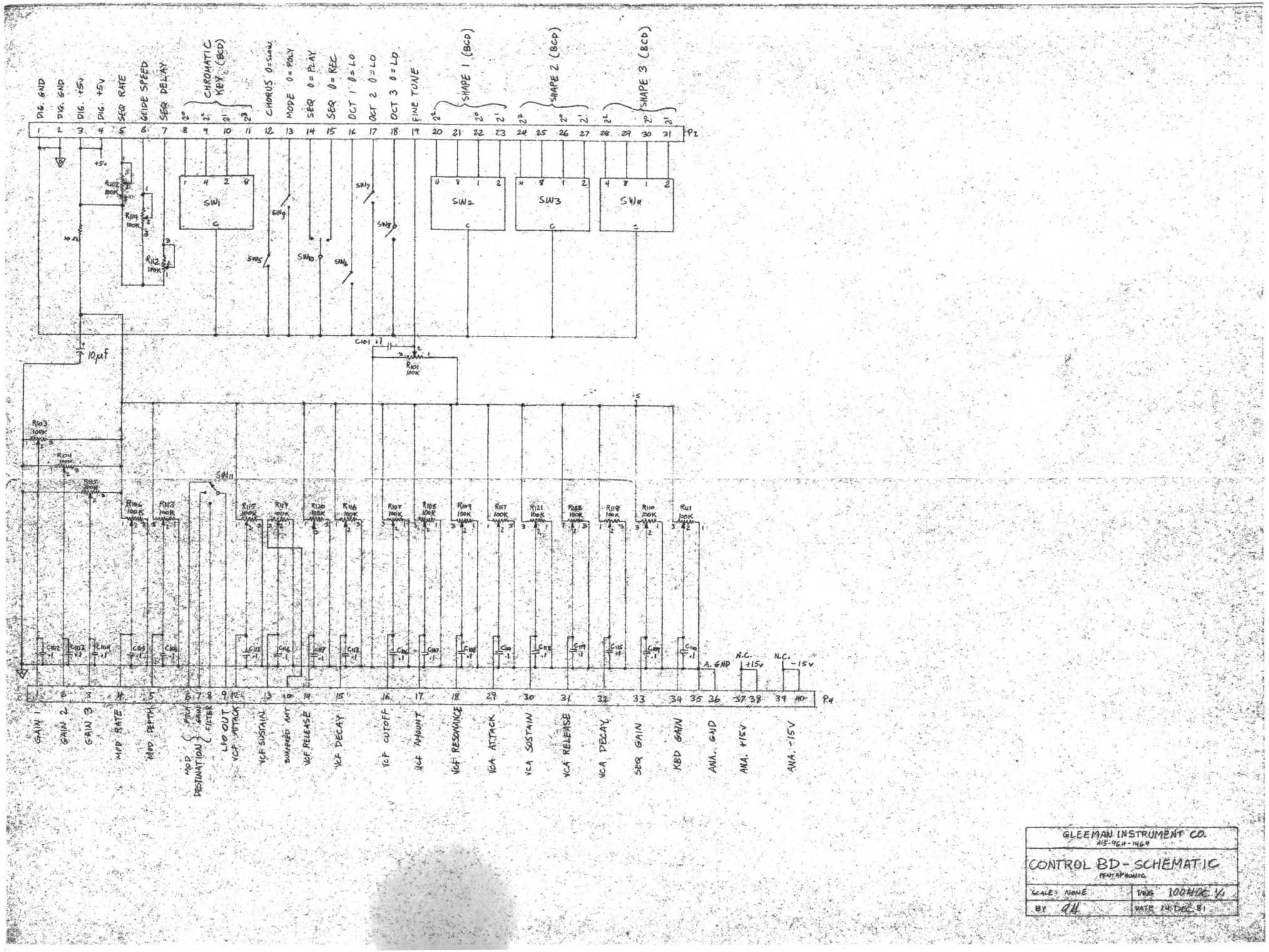
	ID	DESC	VAL	MFG	CODE	
	1	PWB #10042 LATEST REV.		MARTEX	(1)	
80	2	DISPLACEMENT CONNECTOR	3418-0000T	SCOTCH FLEX	(2)	40
	3	RIBBON CABLE	76164-40	BERG	(1)	
	4	DISPLACEMENT CONNECTOR	3417-6000	SCOTCH FLEX	(2)	
	5	SPACER (part of SW5-SW11)			7	
	6	NUT (part of SW5-SW11)			7	

80
12 SWITCH HOLE & MOUNT PRES
4 FEED THRU
349

GLEEMAN INSTRUMENT CO.
415-964-1464

CONTROL BD - ASSY

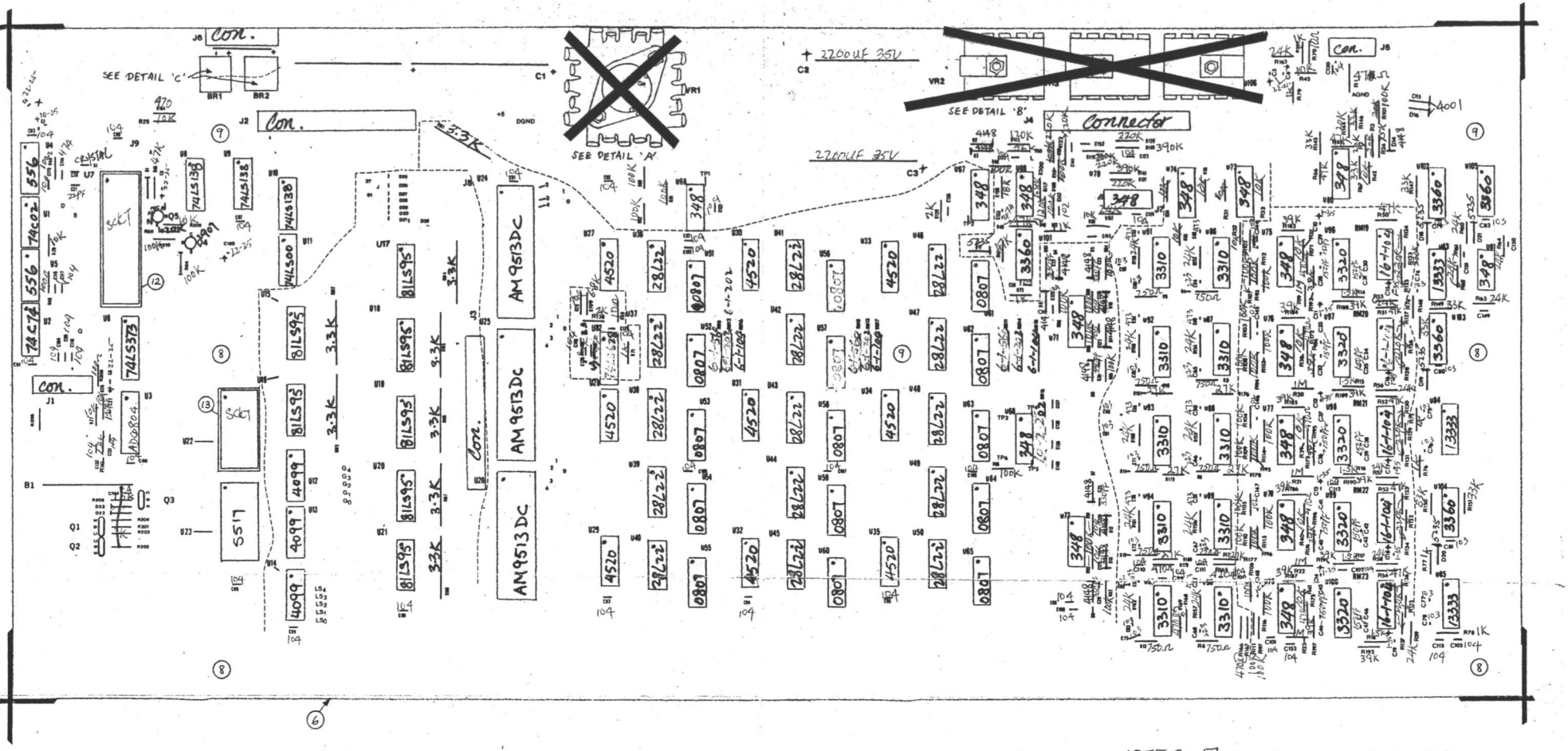
SCALE: 1:1	DWG: 10044G 1/1
BY: ajf	DATE: 15 JUN 82

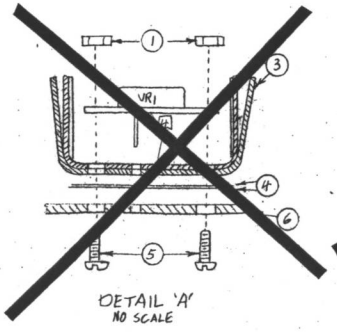


GLEEMAN INSTRUMENT CO.
415-964-1464

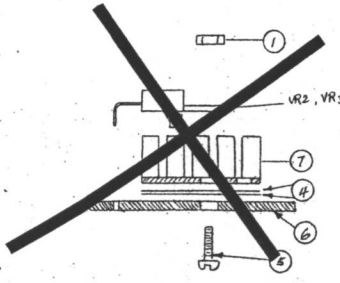
CONTROL BD - SCHEMATIC
PENTAPHONIC

SCALE: NONE	DWG 100HOC 1/1
BY GH	DATE 14 DEC 81

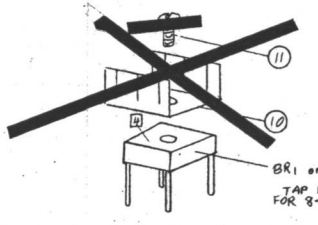




DETAIL 'A'
NO SCALE



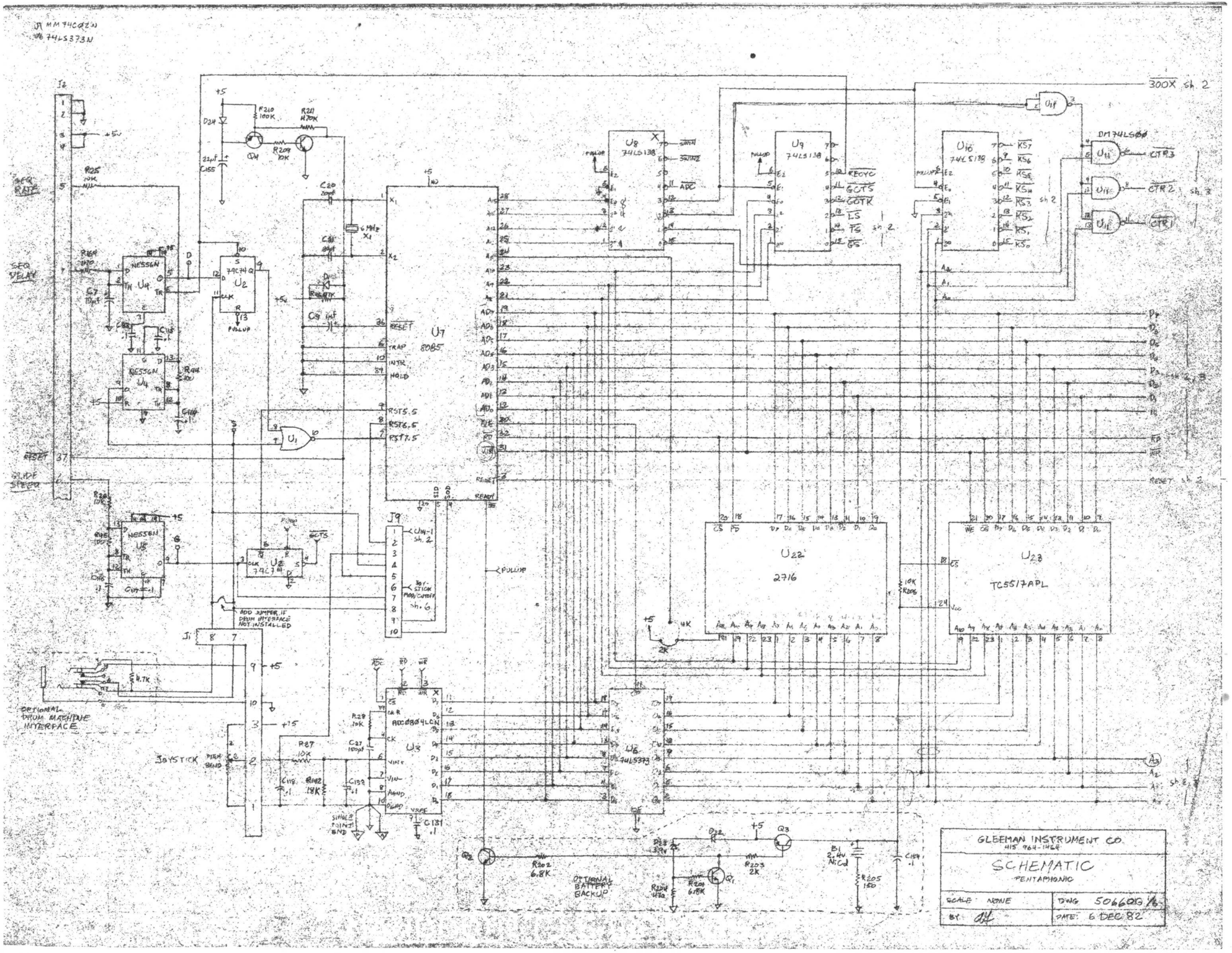
DETAIL 'B'
NO SCALE

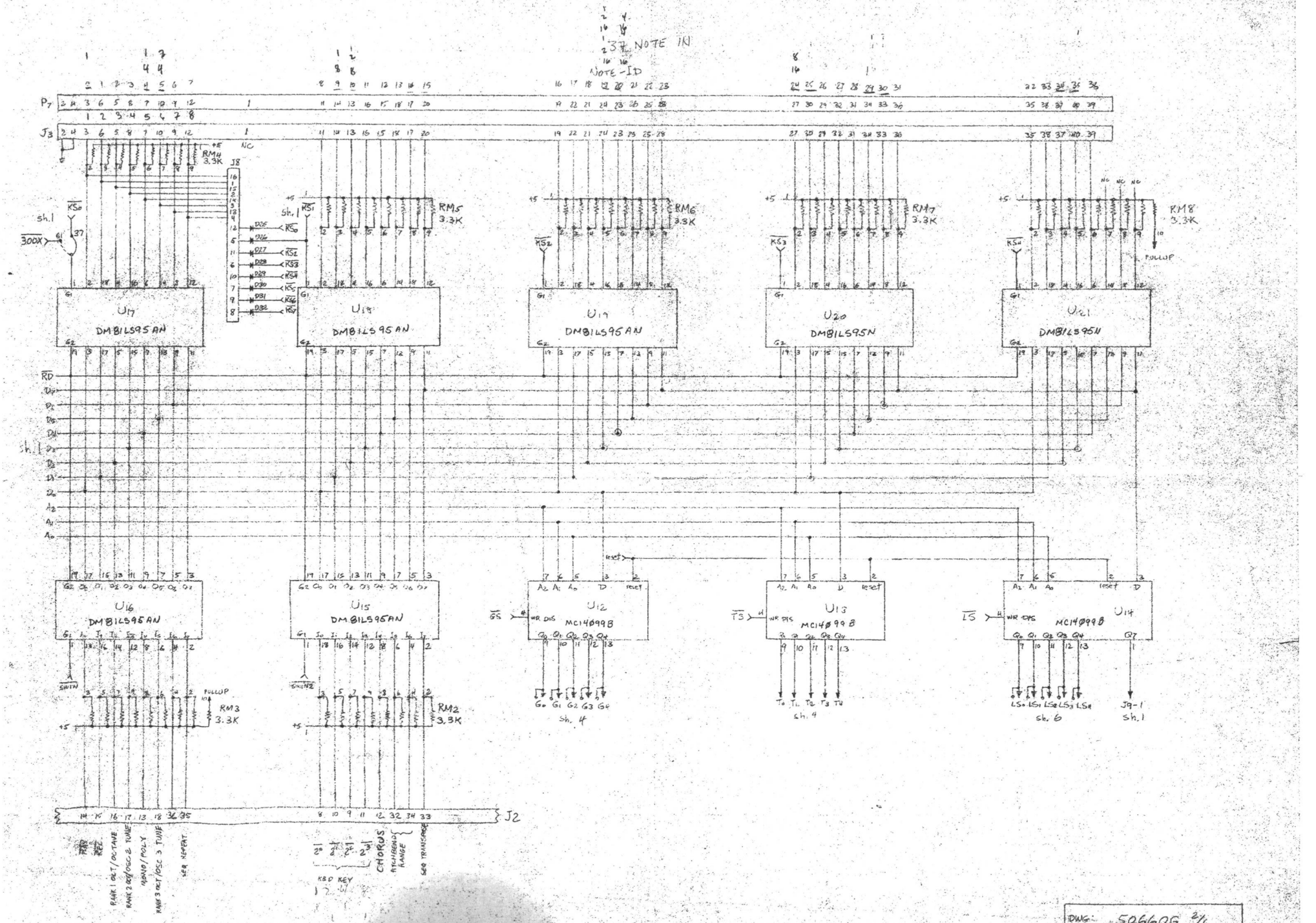


DETAIL 'C'
No SCALE

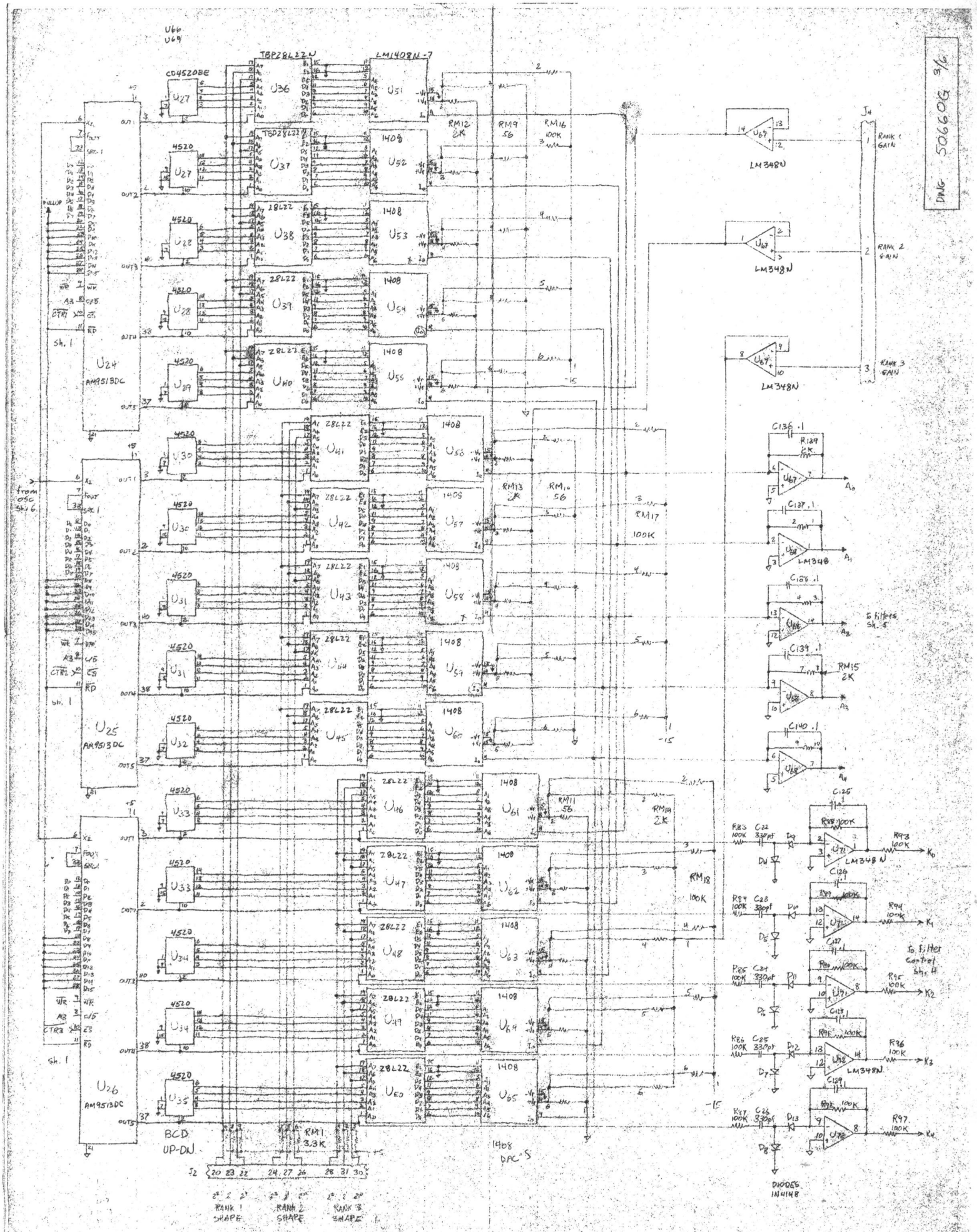
NOTES:
1. SPACERS MUST BE CRIMPED BEFORE SOLDERING. ALL SPACERS TO BE INSTALLED ON THE FOIL (NON-COMPONENT) SIDE OF ITEM 6
2. ALL ICs AND MODULES ARE INSTALLED SO THAT PIN 1 IS IN THE UPPER-LEFT CORNER.
3. AFTER SOLDERING CLEAN ASSY WITH FREON FLUX REMOVER.
4. APPLY EVEN COATING OF THERMAL GREASE ON HEATSINK-MATING SURFACE OF BR1, BR2, VR1, VR2, VR3, AND U106

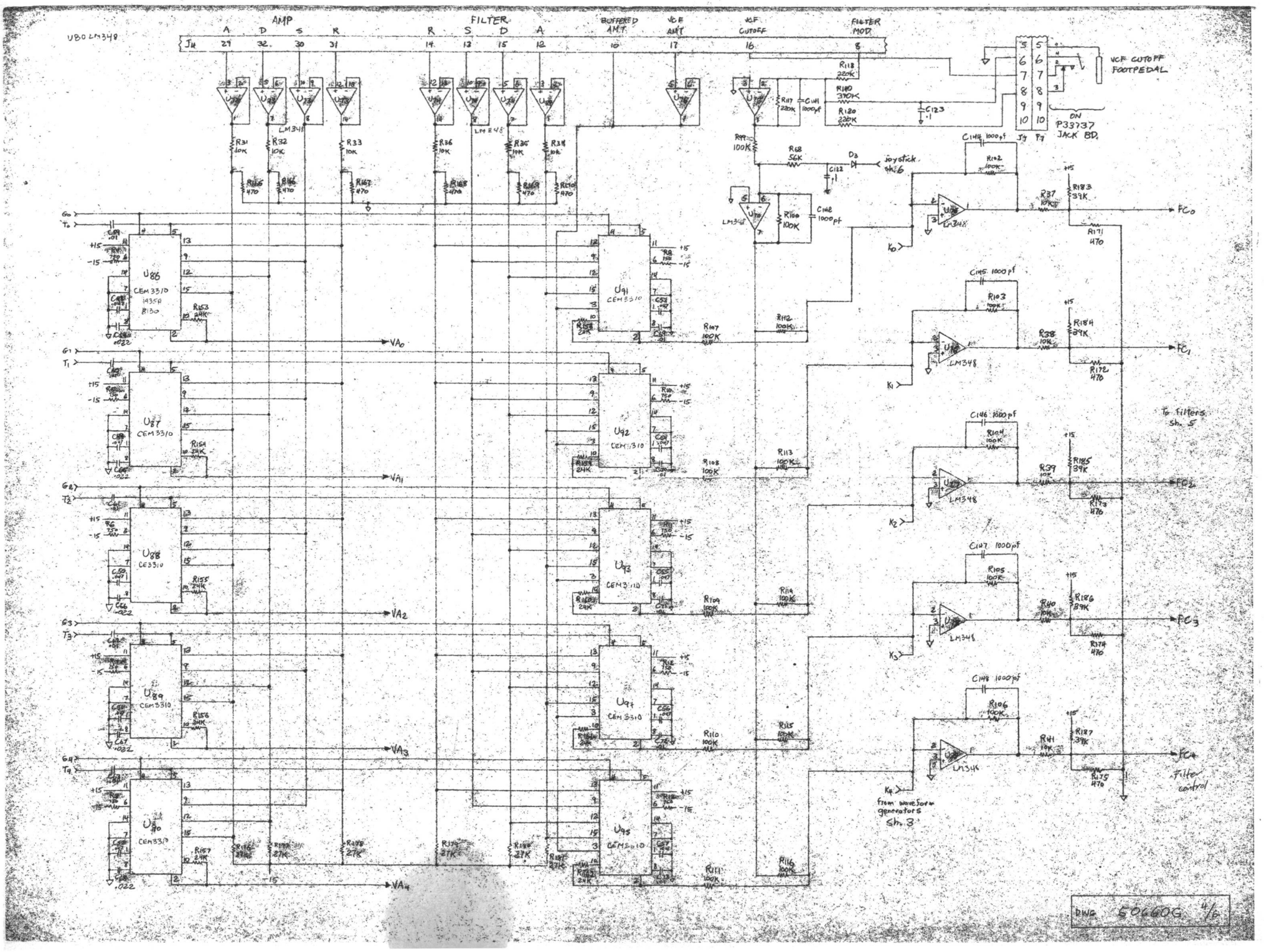
GLEEMAN INSTRUMENTS 415-964-1464	
MAIN BOARD - ASSY	
SCALE 1:1	DWG 506686 1/2
BY [illegible]	DATE 2 NOV 82

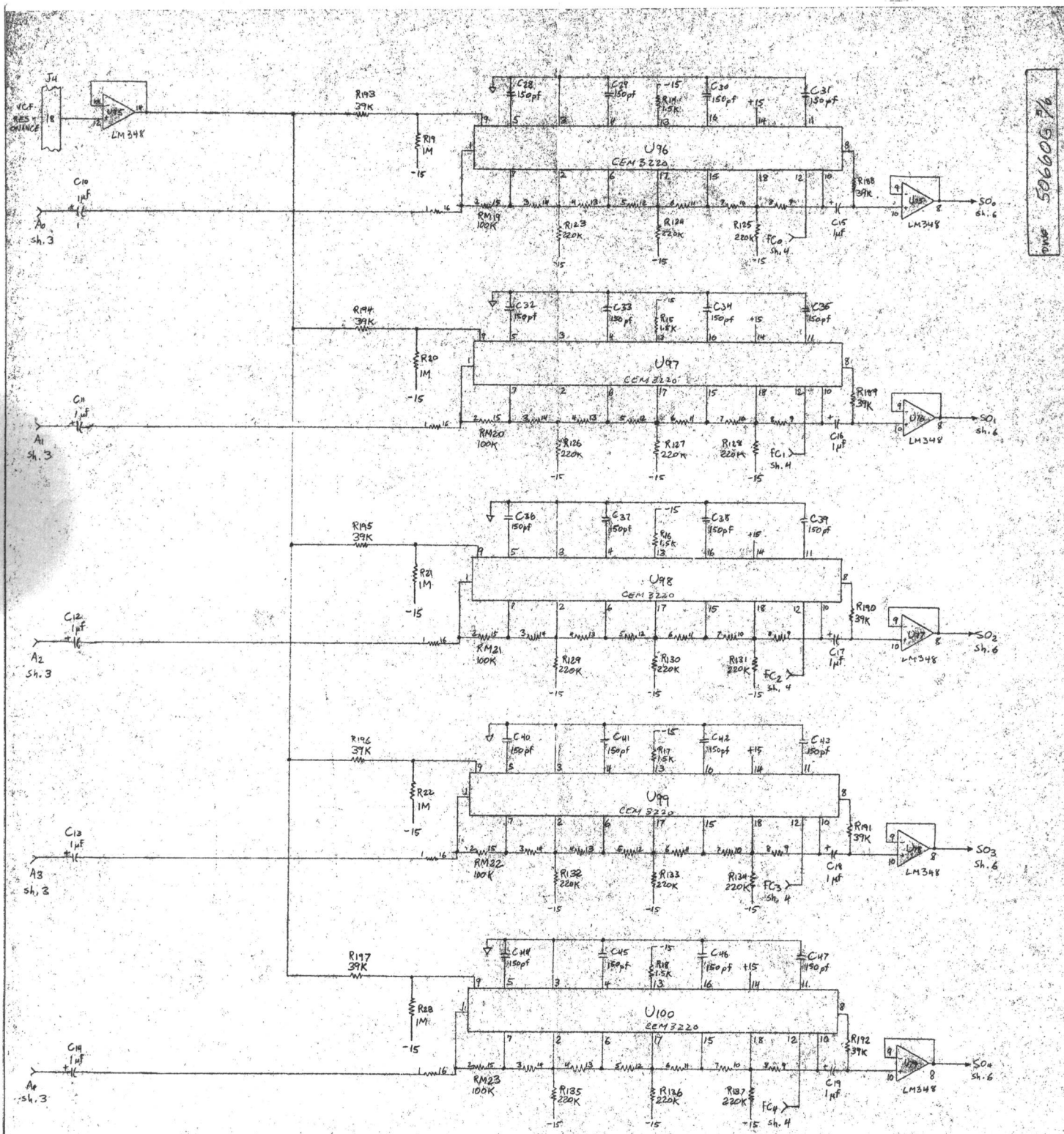

MM74C02N
74LS373N
300X sh 2
SEQ RATE
SEQ DELAY
RESET
SLIDE SPEED
U7 8085
U8 74LS138
U9 74LS138
U16 74LS138
U22 2716
U23 TC5517APL
U6 74LS373
U3 ADC0804LCN
J1
J9
OPTIONAL DRUM MACHINE INTERFACE
JOYSTICK
OPTIONAL BATTERY BACKUP
GLEEMAN INSTRUMENT CO.
SCHEMATIC
PENTAPHONIC
SCALE NONE
DWG 506603
DATE 6 DEC 82

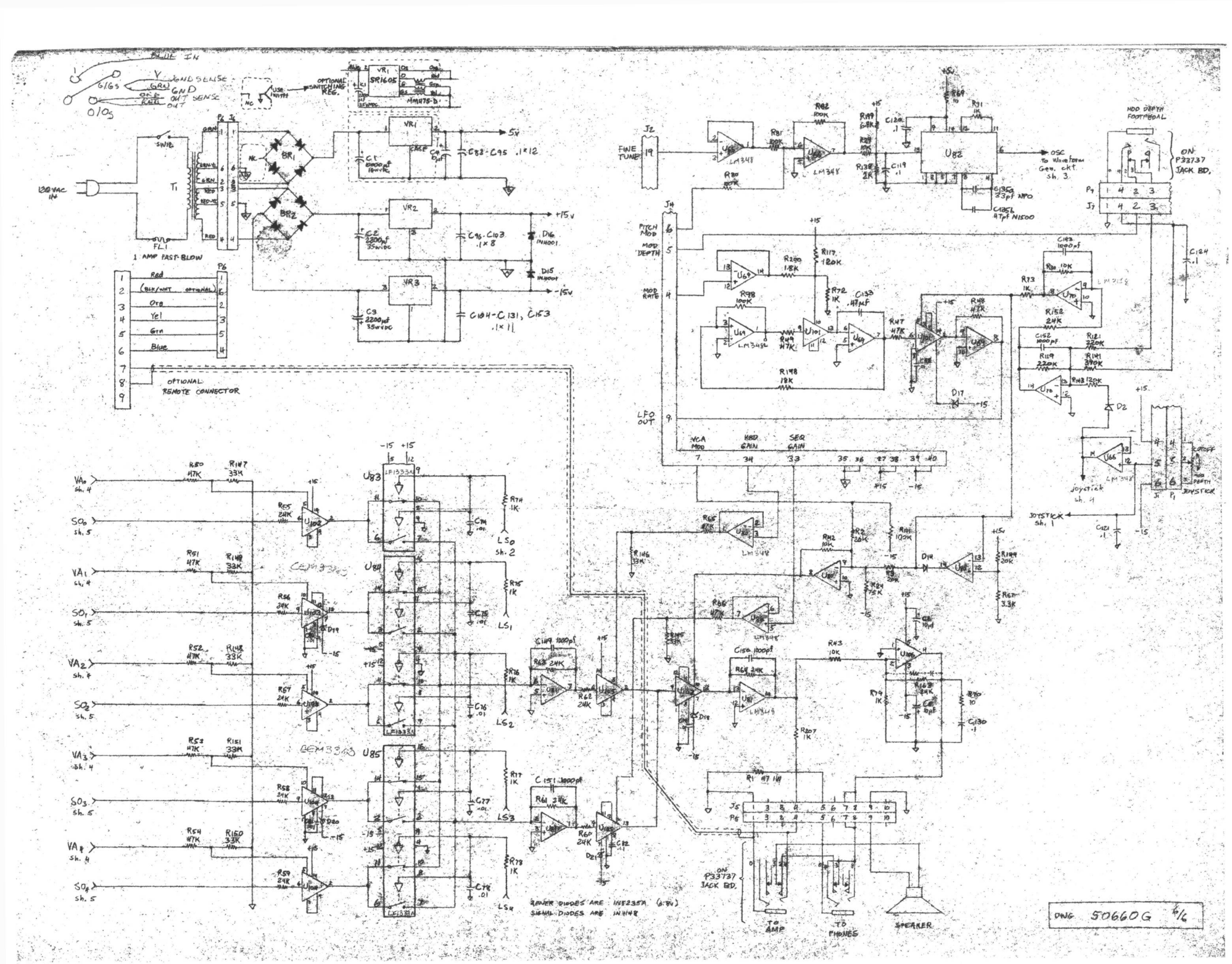


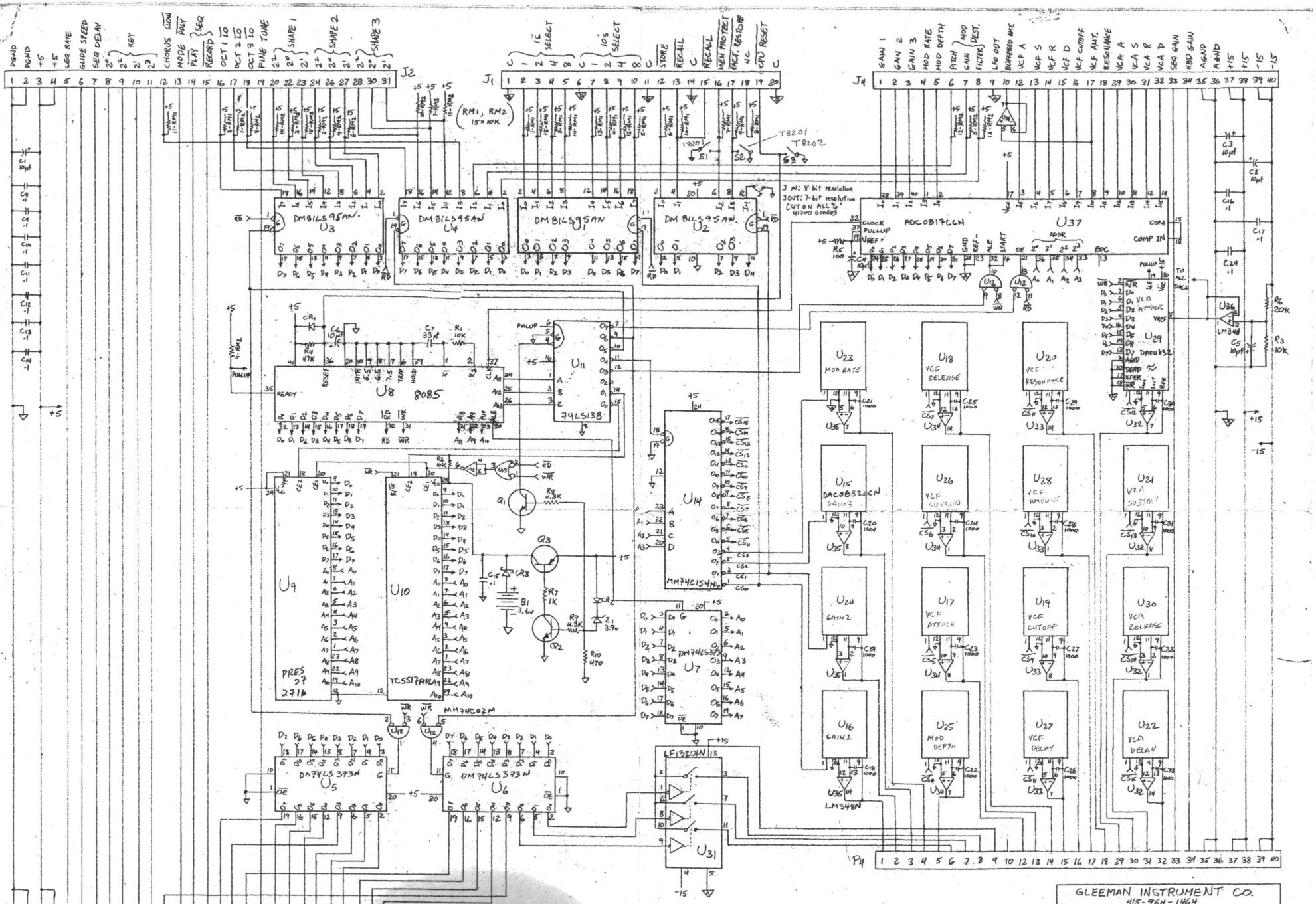
DWG: 506606 2/2

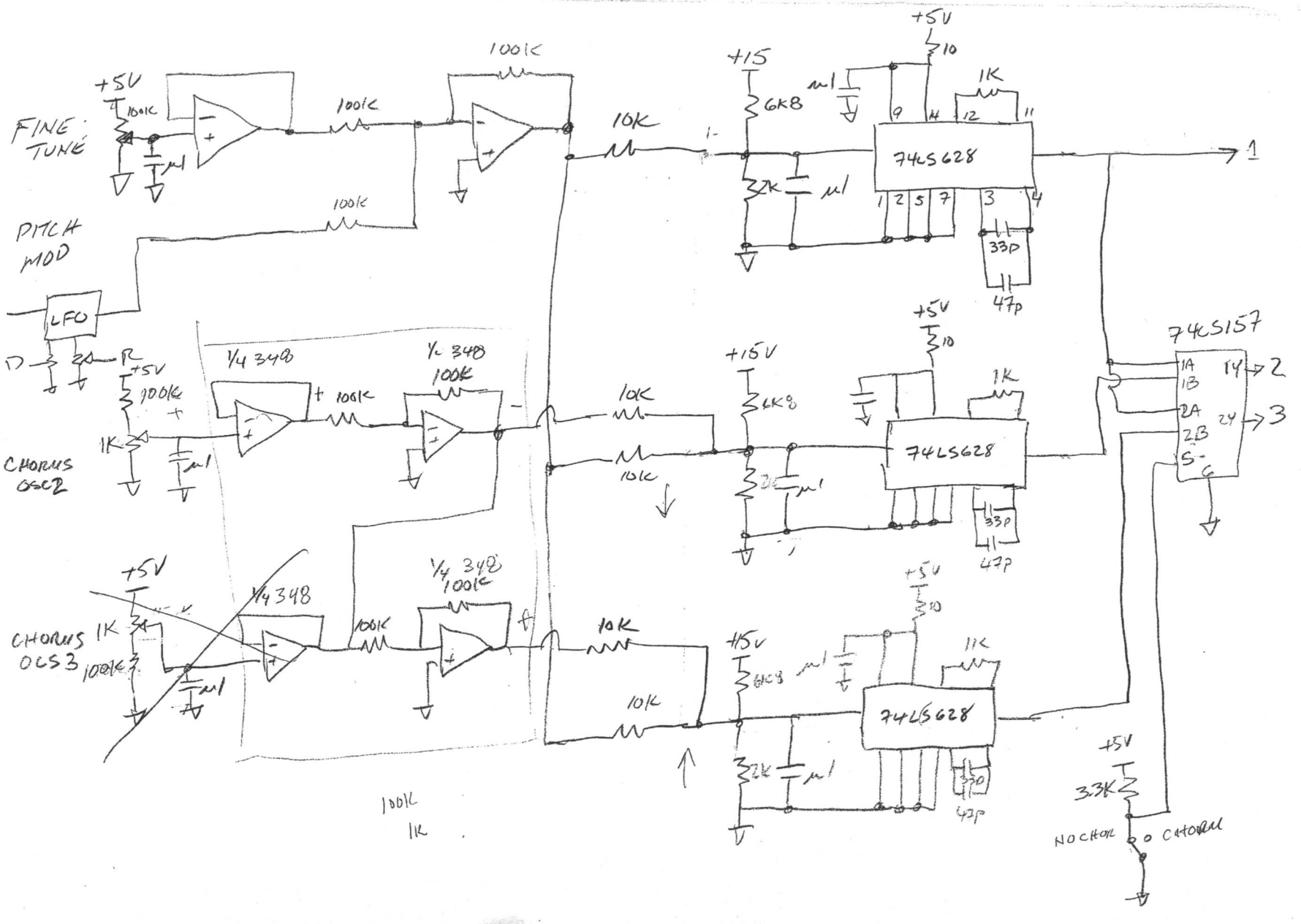

DWG 5066OG 9/6
U24
AM9513DC
U25
AM9513DC
U26
AM9513DC
BCD UP-DN
1408 DAC'S
LM348N
LM348
DIODES IN4148
RANK 1 GAIN
RANK 2 GAIN
RANK 3 GAIN
RANK 1 SHAPE
RANK 2 SHAPE
RANK 3 SHAPE
from osc Sh. 6
to filters Sh. 5
To Filter Control Sh. 4

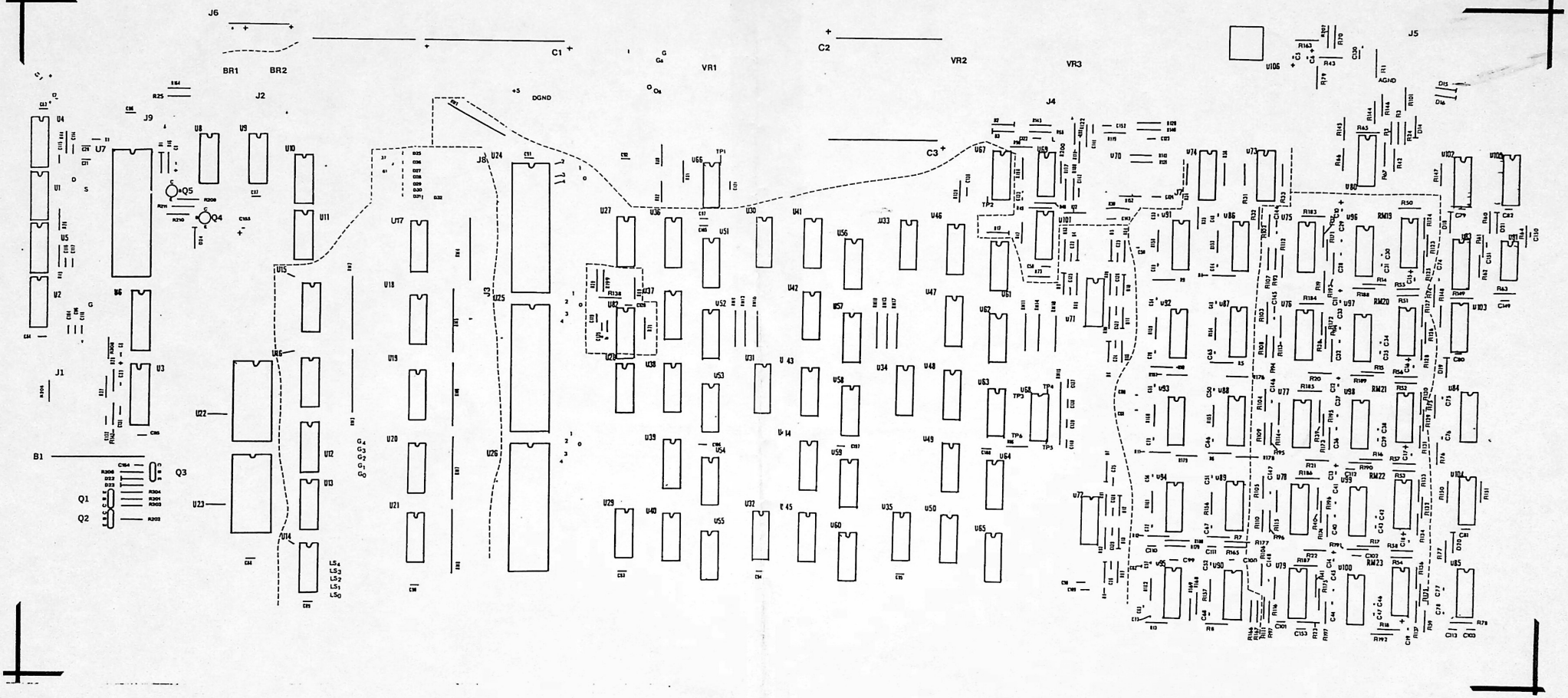

AMP
FILTER
A D S R
R S D A
BUFFERED AMT
VCF AMT
VCF CUTOFF
FILTER MOD
J14
29 32 30 31
14 13 15 12 10 17 16 8
U80 LM348
LM348
R31 10K
R32 10K
R33 10K
R36 10K
R35 10K
R34 10K
R166 470
R165 470
R167 470
R168 470
R169 470
R170 470
R118 220K
R117 220K
C141 1000pf
R120 220K
C123 .1
R119 100K
R116 56K
D3
C122 .1
joystick sh. 6
R180 100K
C148 1000pf
VCF CUTOFF FOOTPEDAL
ON P33737 JACK BD.
J3 P3
C144 1000pf
R182 100K
R183 39K
R37 10K
R171 470
FC0
K0
C145 1000pf
R103 100K
R184 39K
R38 10K
R172 470
FC1
K1
C146 1000pf
R104 100K
R185 39K
R39 10K
R173 470
FC2
K2
C147 1000pf
R105 100K
R186 39K
R40 10K
R174 470
FC3
K3
C148 1000pf
R106 100K
R187 39K
R41 10K
R175 470
FC4
K4
LM348
To filters Sh. 5
Filter control
from waveform generators Sh. 3
G0 T0
G1 T1
G2 T2
G3 T3
G4 T4
U86 CEM3310 1435A 8130
U87 CEM3310
U88 CEM3310
U89 CEM3310
U90 CEM3310
U91 CEM3310
U92 CEM3310
U93 CEM3310
U94 CEM3310
U95 CEM3310
VA0
VA1
VA2
VA3
VA4
+15
-15
DWG 50460G 4/6


J14
VCF RESONANCE
U95
LM348
R193 39K
R19 1M
-15
C28 150pf
C29 150pf
C30 150pf
C31 150pf
R114 1.5K
+15
U96
CEM3220
C10 1μF
A0 sh.3
RM19 100K
R123 220K
R124 220K
R125 220K
FC0 sh.4
C15 1μF
R198 39K
U85
LM348
SO0 sh.6
R194 39K
R20 1M
C32 150pf
C33 150pf
C34 150pf
C35 150pf
R15 1.5K
U97
CEM3220
C11 1μF
A1 sh.3
RM20 100K
R126 220K
R127 220K
R128 220K
FC1 sh.4
C16 1μF
R199 39K
U86
LM348
SO1 sh.6
R195 39K
R21 1M
C36 150pf
C37 150pf
C38 150pf
C39 150pf
R16 1.5K
U98
CEM3220
C12 1μF
A2 sh.3
RM21 100K
R129 220K
R130 220K
R131 220K
FC2 sh.4
C17 1μF
R190 39K
U87
LM348
SO2 sh.6
R196 39K
R22 1M
C40 150pf
C41 150pf
C42 150pf
C43 150pf
R17 1.5K
U99
CEM3220
C13 1μF
A3 sh.3
RM22 100K
R132 220K
R133 220K
R134 220K
FC3 sh.4
C18 1μF
R191 39K
U88
LM348
SO3 sh.6
R197 39K
R23 1M
C44 150pf
C45 150pf
C46 150pf
C47 150pf
R18 1.5K
U100
CEM3220
C14 1μF
A4 sh.3
RM23 100K
R135 220K
R136 220K
R137 220K
FC4 sh.4
C19 1μF
R192 39K
U89
LM348
SO4 sh.6
5960695 Rev


BLUE IN
GRN
GND SENSE
GND
OUT SENSE
OUT
0105
SW1
T1
120 VAC IN
FL1
1 AMP FAST-BLOW
BR1
BR2
VR1
SR1605
OPTIONAL SWITCHING REG.
+5V
+15V
-15V
P6
Red
Org
Yel
Grn
Blue
OPTIONAL REMOTE CONNECTOR
FINE TUNE
OSC to Waveform Gen. ckt sh. 3.
MOD DEPTH FOOTPEDAL
ON P33737 JACK BD.
PITCH MOD
MOD DEPTH
MOD RATE
LFO OUT
VCA MOD
KBD GAIN
SER GAIN
JOYSTICK sh. 1
JOYSTICK
VA0 sh. 4
SO0 sh. 5
VA1 sh. 4
SO1 sh. 5
VA2 sh. 4
SO2 sh. 5
VA3 sh. 4
SO3 sh. 5
VA4 sh. 4
SO4 sh. 5
LS0 sh. 2
LS1
LS2
LS3
LS4
CEM3340
LF13334
ZENER DIODES ARE IN5235A (6.8V)
SIGNAL DIODES ARE IN4148
ON P33737 JACK BD.
TO AMP
TO PHONES
SPEAKER
DWG 50660G 6/6


J2
J1
J4
P2
P4
U3
U4
U2
U37
U8 8085
U11
74LS138
U14
MM74C154N
U7
DM74LS373N
U5
U6
U9
U10
U18
U18
MM74C02M
U31
LF13201N
U23 MOD RATE
U18 VCF RELEASE
U20 VCF RESONANCE
U15 DAC0832LCN GAIN3
U26 VCF SUSTAIN
U28 VCF AMOUNT
U21 VCA SUSTAIN
U24 GAIN2
U17 VCF ATTACK
U19 VCF CUTOFF
U30 VCA RELEASE
U16 GAIN1
U25 MOD DEPTH
U27 VCF DELAY
U22 VCA DELAY
LM348N
U36 LM348
U29 DAC0832
ADC0817CCN
PRES 27 2716
TC5517APAL1
Q1
Q2
Q3
B1 3.6V
CR1
CR2
CR3
Z1 3.9V
S1
S2
S3
T8201
T8202
(RM1, RM2 15x 10K)
GLEEMAN INSTRUMENT CO.
HIS-96H-1464
PRESETTER-SCHEM.
SCALE: NONE
DWG. 41690A V1
BY: AM
DATE: 15 JUN 82
TIF 42.


FINE TUNE
+5V
100K
100K
100K
PITCH MOD
LFO
1/4 348
1/4 348
100K
CHORUS OSC2
1K
1/4 348
1/4 348
100K
CHORUS OSC3
1K
100K
100K
1K
10K
10K
10K
+15
6K8
2K
74LS628
+5V
10
1K
33P
47P
74LS157
1A
1B
2A
2B
S
1Y
2Y
2
3
3.3K
NO CHOR
CHORUS


J6
BR1
BR2
C1
VR1
C2
VR2
VR3
J5
J2
J9
J8
J4
C3
DGND
AGND
U1
U2
U3
U4
U5
U6
U7
U8
U9
U10
U11
U12
U13
U14
U15
U16
U17
U18
U19
U20
U21
U22
U23
U24
U25
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U27
U28
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U91
U92
U93
U94
U95
U96
U97
U98
U99
U100
U101
U102
U103
U104
U105
U106
Q1
Q2
Q3
Q4
Q5
B1
TP1
TP2
TP3
TP4
TP5
TP6
RM19
RM20
RM21
RM22
RM23
JU1

PROBLEM: 1 OSCILLATOR OF 3 OUT, ALL 5 VOICES

1 Clock Generator. Verify presence of TTL squarewaves at Clock Generator (U24-U26) pins 3,2,40,38,37. Loss indicates bad Clock Gen.

2 Gain Buffer. Verify presence of Gain control voltage (0-5VDC) at pertinent Gain Buffer (U67 pins 1,8,or 14). Loss indicates bad buffer or bad signal from Presetter.

PROBLEM: 1 VOICE OUT ON 1 OSCILLATOR

Determine which voice out of 5 is out (see procedure in "... 1 VOICE OF 5 OUT..."). Determine which Oscillator the bad voice is on, then locate the pertinent Clock Generator (U24-U26), Divider (U27-U35), Wave ROM (U36-U50), and DAC (U51-U65) for the following tests.

1 Clock Generator. Verify presence of TTL squarewave at pertinent Clock Generator output. Loss indicates bad Clock Gen.

2 Divider. Verify TTL squarewaves at the pertinent Divider outputs (pins 3,4,5,6 or 11,12,13,14). Loss indicates bad divider.

3 ROM. Verify TTL pulses at pertinent Wave ROM (pins 6,7, 8,9,11,12). Loss indictaes bad ROM.

4 DAC. Correct operation of the DAC is difficult to verify. If the pertinent Clock Generator, Divider, and ROM are good, the DAC is bad by default.

PROBLEM: NO SEQUENCER OUTPUT

1 Sequencer Rate Clock. Verify TTL pulses at U4 pin 9. Absence indicates bad U4, associated circuitry, or no control signal from Presetter (indicated by 0VDC at U4 pin 1).

2 Seq. Interrupt. Verify TTL pulses at U2 pin 11. Absence indicates bad Drum Sync jack. Verify 0VDC at U2 pin 12 2V+ indicates bad U4. Verify TTL pulses at U2 pin 9. Absence indicates bad U2.

3 Voice Routing. Play back a polyphonic sequence and verify 2.4V+ at U14 pins 9,10,11,12,13. Stuck-at-zero indicates bad U14.

4 Seq. Gain Buffer. Verify Sequencer Gain control action at U80 pin 7 (0-5VDC). Stuck-at-zero indicates bad U80 or no signal from Presetter.

5 Seq. Summing Amp. Play back a sequence and verify audio at U81 pin 1. Absence indicates bad U81.

PROBLEM: NO OUTPUT AT ALL

1 Power. +5.0±0.05VDC Measure at U7 pin 40
+15.0±0.20 VDC Measure at D16 cathode
-15.0±0.20 VDC Measure at D15 anode. Loss of +5V will probably be due to failure of VR1. Loss of ±15V may be due to failure of Tantalum caps (try C5 or C6 first) Replace with aluminum electrolytic type.

2 Micro. Verify 6.00MHz at U7 pin 2. Wrong freq Indicates bad crystal X1 or U7. Verify 3.00MHz TTL squarewave at U7 pin 37. Loss indicates bad U7. Verify random TTL activity at U7 pins 30,31,32. Loss indicates failure of micro section. Contact factory. Verify 4V+ at U7 pin 35. Low V indicates bad LSTTL inputs at U8,U9,U10.

3 Connectors. Verify all correctly mated. Note J6 is easily mismated.

4 Master VCO. Verify 6MHz at U82 pin 6 which varies ±0.5 MHz with Fine Tune control. Replacing U82 may necessitate changing R71 to obtain 6.00MHz when control is at "5".

5 Output Preamp. Verify both keyboard and sequencer audio at U81 pin 14. Loss indicates bad U81.

6 Power Amp. Verify audio at U106 pin 4. Loss indicates bad U106.

PROBLEM: 1 VOICE OF 5 OUT, ALL 3 OSCILLATORS

Determine which voice is out by powering off then back on. Play keyboard 1 note at a time in POLY mode and count keys from 1 to 5. The number of the key producing no sound is the bad voice ("n").

1 Voice n Sum. Verify audio at the pertinent summing amp (U67-7, U68-1, U68-14, U68-8, U68-7). Loss indicates bad summing amp, or sometimes a bad DAC (U51-U65) will hold off the other two for that voice.

2 Filter n Control. Verify Cutoff control and envelope action at filter n Control Amp (U75-U79) pin 1. (0 to -2V DC). Loss could stop filter action, indicates bad amp.

3 Filter n. Verify audio at filter output (U96-U100) pin 10. Loss indicates bad filter.

4 Filter n Buffer. Verify audio at filter n Buffer (U75-U79) pin 8. Loss indicates bad buffer.

5 Amp n Envelope. Verify ADSR envelope at Amp n Envelope Generator (U86-U90) pin 2 when key is played. Loss indicates bad Envelope Gen.

6 VCA Sum. Verify audio at Keyboard Summing Amp U81 pin 7 when key is played. Loss could be due either to bad VCA (U102-U104) or bad Routing Switch (U83-U85). If voice is present for sequences but not keyboard notes, especially if a click is present, the Routing Switch is bad. If voice is absent for both keyboard and se-

Desig	Test Pins	Signal	Other Causes of Failure
U1	10	Sequencer Interrupt	U2, U4
U2	9	Ext. Sync Latch	Drum Jack, U4, U9
	6	Glide Interrupt	U5, U9
U3	19	ADC Clock	R28, C27
U4	5(D)	Seq. Delay Timer	Delay Control, R164, C7
	9(S)	Seq. Rate Clock	Rate Control, R44, C114
U5	9(G)	Glide Speed Clk	Glide Control, R26
U6	2,5, 6,9, 12,	Address Latch	U7
	15,16,19		
U7	2	Crystal Clock 6MHz	X1, C21
	31	$\overline{\text{Write}}$ Signal	U6, U22, U23
	32	$\overline{\text{Read}}$ Signal	U6, U22, U23
	30	ALE Signal	X1, C21
	36	Power On Reset	Q4, Q5
	35	Pullup +5VDC	Q2, RM3, U8, U9, U10
	37	3MHz Clock	X1, C21
U8	7	$\overline{\text{SWIN}}$ Chip Select	U7
	9	$\overline{\text{SWIN2}}$ Chip Select	
	11	$\overline{\text{ADC}}$ Select	
	12	$\overline{\text{300X}}$ Select	
	13	$\overline{\text{Counter}}$ Select	
	14	$\overline{\text{RAM}}$ Select	
	15	$\overline{\text{ROM}}$ Select	
U9	10	$\overline{\text{RECYC}}$ Trigger	U7, U8
	11	GCTS Interrupt Reset	
	13	$\overline{\text{LS}}$ Chip Select	
	14	$\overline{\text{TS}}$ Chip Select	
	15	$\overline{\text{GS}}$ Chip Select	
U10	7	$\overline{\text{KS7}}$ Chip Sel	U7, U8
	9	$\overline{\text{KS6}}$ Chip Sel	
	10	$\overline{\text{KS5}}$ Chip Sel	
	11	$\overline{\text{KS4}}$ Chip Sel	
	12	$\overline{\text{KS3}}$ Chip Sel	
	13	$\overline{\text{KS2}}$ Chip Sel	
	14	$\overline{\text{KS1}}$ Chip Sel	
	15	$\overline{\text{KS0}}$ Chip Sel	
U11	3	200X Inverter	U6, U7, U8
	6	$\overline{\text{CTR3}}$ Chip Sel	
	8	$\overline{\text{CTR2}}$ Chip Sel	
	11	$\overline{\text{CTR1}}$ Chip Sel	
U12	9	Gate 1	U6, U8
	10	Gate 2	
	11	Gate 3	
	12	Gate 4	

Desig	Test Pins	Signal	Other Causes of Failure
U13	9	Trigger 1	U6, U8
	10	Trigger 2	
	11	Trigger 3	
	12	Trigger 4	
	13	Trigger 5	
U14	9	Switch 1	U6, U8
	10	Switch 2	
	11	Switch 3	
	12	Switch 4	
	13	Switch 5	
U15	-	Buffer, Trans/Chorus	U8, Presetter
U16	-	Buffer, Modes/Octave	U8, Presetter
U17	-	Buffer, KBD 0-7	Keyboard, U10
U18	-	Buffer, KBD 8-15	Keyboard, U10
U19	-	Buffer, KBD 16-23	Keyboard, U10
U20	-	Buffer, KBD 24-31	Keyboard, U10
U21	-	Buffer, KBD 32-36	Keyboard, U10
U22	-	Program EPROM	U6, U7, U8
U23	-	Data RAM	U6, U7, U8
U24	3	Osc 1 Voice 1 Clk	U11, U82
	2	1 2	
	40	1 3	
	38	1 4	
	37	1 5	
U25	3	Osc 2 Voice 1	U11, U82
	2	2 2	
	40	2 3	
	38	2 4	
	37	2 5	
U26	3	Osc 3 Voice 1	U11, U82
	2	3 2	
	40	3 3	
	38	3 4	
	37	3 5	
U27	3	U24-3 /2	U24
	4	U24-3 /4	
	5	U24-3 /8	
	6	U24-3 /16	
	11	U24-2 /2	
	12	U24-2 /4	
	13	U24-2 /8	
	14	U24-2 /16	
U28	3	U24-40 /2	U24
	4	U24-40 /4	
	5	U24-40 /8	

DIVIDERS

Desig	Test Pins	Signal	Other Causes of Failure
U28	11	U24-38 /2	U24
	12	U24-38 /4	
	13	U24-38 /8	
	14	U24-38 /16	
U29	3	U24-37 /2	U24
	4	U24-37 /4	
	5	U24-37 /8	
	6	U24-37 /16	
U30	3	U25-3 /2	U25
	4	U25-3 /4	
	5	U25-3 /8	
	6	U25-3 /16	
	11	U25-2 /2	
	12	U25-2 /4	
	13	U25-2 /8	
	14	U25-2 /16	
U31	3	U25-40 /2	U25
	4	U25-40 /4	
	5	U25-40 /8	
	6	U25-40 /16	
	11	U25-38 /2	
	12	U25-38 /4	
	13	U25-38 /8	
	14	U25-38 /16	
U32	3	U25-37 /2	U25
	4	U25-37 /4	
	5	U25-37 /8	
	6	U25-37 /16	
U33	3	U26-3 /2	U26
	4	U26-3 /4	
	5	U26-3 /8	
	6	U26-3 /16	
	11	U26-2 /2	
	12	U26-2 /4	
	13	U26-2 /8	
	14	U26-2 /16	
U34	3	U26-40 /2	U26
	4	U26-40 /4	
	5	U26-40 /8	
	6	U26-40 /16	
	11	U26-38 /2	
	12	U26-38 /4	
	13	U26-38 /8	
	14	U26-38 /16	
U35	3	U26-37 /2	U26
	4	U26-37 /4	

Desig	Test Pins	Signal	Other Causes of Failure
U36	6,7,8 9,11,12	Osc 1 Voice 1 Wave ROM	U24, U27, Presetter
U37	6,7,8 9,11,12	Osc 1 Voice 2 Wave ROM	U24, U27, Presetter
U38	6,7,8 9,11,12	Osc 1 Voice 3 Wave ROM	U24, U28, Presetter
U39	6,7,8 9,11,12	Osc 1 Voice 4 Wave ROM	U24, U28, Presetter
U40	6,7,8 9,11,12	Osc 1 Voice 5 Wave ROM	U24, U29, Presetter
U41	6,7,8 9,11,12	Osc 2 Voice 1 Wave ROM	U25, U30, Presetter
U42	6,7,8 9,11,12	Osc 2 Voice 2 Wave ROM	U25, U30, Presetter
U43	6,7,8 9,11,12	Osc 2 Voice 3 Wave ROM	U25, U31, Presetter
U44	6,7,8 9,11,12	Osc 2 Voice 4 Wave ROM	U25, U31, Presetter
U45	6,7,8 9,11,12	Osc 2 Voice 5 Wave ROM	U25, U32, Presetter
U46	6,7,8 9,11,12	Osc 3 Voice 1 Wave ROM	U26, U33, Presetter
U47	6,7,8 9,11,12	Osc 3 Voice 2 Wave ROM	U26, U33, Presetter
U48	6,7,8 9,11,12	Osc 3 Voice 3 Wave ROM	U26, U34, Presetter
U49	6,7,8 9,11,12	Osc 3 Voice 4 Wave ROM	U26, U34, Presetter
U50	6,7,8 9,11,12	Osc 3 Voice 5 Wave ROM	U26, U35, Presetter
U51	-	Osc 1 Voice 1 DAC	U36
U52	-	Osc 1 Voice 2 DAC	U37
U53	-	Osc 1 Voice 3 DAC	U38
U54	-	Osc 1 Voice 4 DAC	U39
U55	-	Osc 1 Voice 5 DAC	U40
U56	-	Osc 2 Voice 1 DAC	U41
U57	-	Osc 2 Voice 2 DAC	U42
U58	-	Osc 2 Voice 3 DAC	U43
U59	-	Osc 2 Voice 4 DAC	U44
U60	-	Osc 2 Voice 5 DAC	U45
U61	-	Osc 3 Voice 1 DAC	U46
U62	-	Osc 3 Voice 2 DAC	U47
U63	-	Osc 3 Voice 3 DAC	U48
U64	-	Osc 3 Voice 4 DAC	U49
U65	-	Osc 3 Voice 5 DAC	U50
	1	Fine Tune Buffer	Presetter

Desig	Test Pins	Signal	Other Causes of Failure
U67	1	Osc 2 Gain Buffer	Presetter
	7	Voice 1 Sum	U51, U56, U61
	8	Osc 3 Gain Buffer	Presetter
	14	Osc 1 Gain Buffer	Presetter
U68	1	Voice 2 Sum	U52, U57, U62
	7	Voice 5 Sum	U55, U60, U65
	8	Voice 4 Sum	U54, U59, U64
	14	Voice 3 Sum	U53, U58, U63
U69	1	LFO Hysteresis	U101
	7	LFO Integrator	U101
	8	LFO Buffer	U101
	14	Mod Rate Buffer	Presetter
U70	1	Filter Mod Sum 1	Cutoff Footpedal
	7	Filter Mod Sum 2	U66, D3
	8	Mod Depth Sum 2	
	14	Mod Depth Sum 1	U66, D2
U71	1	Voice 1 F-V	U61, D4, D9
	8	Voice 3 F-V	U63, D6, D11
	14	Voice 2 F-V	U62, D5, D10
U72	8	Voice 5 F-V	U65, D8, D13
	14	Voice 4 F-V	U64, D7, D12
U73	1	Amp Attack Buffer	Presetter
	7	Amp Decay Buffer	
	8	Amp Sustain Buffer	
	14	Amp Release Buffer	
U74	1	Filt Attack Buffer	Presetter
	7	Filt Decay Buffer	
	8	Filt Sustain Buffer	
	14	Filt Release Buffer	
U75	1	Filter 1 Control	U91
	8	Filter 1 Buffer	U96
	14	Resonance Buffer	Presetter
U76	1	Filter 2 Control	U92
	7	Amount Buffer	Presetter
	8	Filter 2 Buffer	U97
U77	1	Filter 3 Control	U93
	8	Filter 3 Buffer	U98
U78	1	Filter 4 Control	U94
	8	Filter 4 Buffer	U99
U79	1	Filter 5 Control	U95
	8	Filter 5 Buffer	U100
U80	1	Keybd Gain Buffer	Presetter
	7	Seq. Gain Buffer	Presetter
	8	Amp Mod Sum	D14, U70
	14	Amp Mod Clamp +2VDC	U70
	1	Seq. Out Sum	U83, U84, U85

Desig	Test Pins	Signal	Other Causes of Failure
U82	6	Master VCO 6MHz	U66
U83	-	Voice 1 Routing	U14, U102
U84	-	Voice 2 Routing	U14, U103
		Voice 3 Routing	
U85	-	Voice 4 Routing	U14, U104
		Voice 5 Routing	
U86	2	Amp 1 Envelope	
U87	2	Amp 2 Env.	
U88	2	Amp 3 Env.	U73, U12, U13
U89	2	Amp 4 Env.	
U90	2	Amp 5 Env.	
U91	2	Filt 1 Envelope	
U92	2	Filt 2 Env.	
U93	2	Filt 3 Env.	U74, U12, U13
U94	2	Filt 4 Env.	
U95	2	Filt 5 Env.	
U96	10	Filter 1	U67
U97	10	Filter 2	U68
U98	10	Filter 3	U68
U99	10	Filter 4	U68
U100	10	Filter 5	U68
U101	-	LFO Rate	U69
		LFO Depth	U69, U70
U102	-	Voice 1 VCA	U75, U86
		Final VCA	U105
U103	-	Voice 2 VCA	U76, U87
		Voice 3 VCA	U77, U88
U104	-	Voice 4 VCA	U78, U89
		Voice 5 VCA	U79, U90
U105	-	Keybd Amp Mod	U81
		Seq. Amp Mod	
U106	4	Power Amp Out	U81

PROBLEM: NO MODULATION

1 Mod Depth Summing Amp. Verify Mod Depth control voltag at U70 pin 8 which varies with joystick and control knob activity. Absence indicates bad U70 or bad control.

2 Mod Rate Buffer. Verify Mod Rate control voltage at U pin 10 (0-2VDC). Voltage out of this range indicate bad U69 or no signal from Presetter.

3 LFO Hysteresis. Verify U69 pin 1 is either +12V or -1 Voltages in between indicate bad U69.

4 LFO Integrator. Verify triangular waveform at U69 pin Voltage beyond ±12VDC indicates bad U69. Voltage

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SERVICE BULLETIN

INSTALLATION OF INTERVAL-TUNING MODIFICATION
Pentaphonic 8110 Series

PREPARE WORKSPACE

You will need at least a 24" X 30" area on your workbench or tabletop. Spread a clean terrycloth towel over the surface to protect the Pentaphonic case.

REQUIRED TOOLS

Large Phillips screwdriver
24-pin IC removal tool
24-pin IC insertion tool
X-ACTO or similar knife

UNPLUG THE PENTAPHONIC

Although there are no exposed high-voltage conductors in the Pentaphonic, it never hurts to play safe. Installation of the Interval-Tuning Modification requires the Upper Assembly to rock back against the back surface. This often causes the actuation of the Power switch. Unpremeditated application of power during the installation of electronic circuitry is never desirable and easily prevented.

OPEN UNIT Fig. 1.

Using a large Phillips screwdriver remove ten 10-32 X 3/4 screws (8-32 in Clear models) from around the perimeter of the Unit. Do not remove the seven 8-32 screws which are also on the bottom but located well inside the perimeter.

When all ten screws have been removed hold the top and bottom together to prevent their uncontrolled separation. Place the Unit in the middle of the workspace in a normal playing position. Raise the back of the case a few inches, then slide it forward until the forward edge clears the keyboard. Raise the forward edge and lower the back until the Upper Assembly rests on its back.

Demate the two large 40-pin ribbon connectors J2 and J4. Demate the 6-pin power connector J6 and the three 10-pin ribbon connectors J1, J5, and J7. Set aside the Lower Assembly temporarily.

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PRESETTER BOARD MODIFICATION Fig. 2.

Using a 24-pin IC removal tool pull out U9 from its socket.

Using a 24-pin IC insertion tool replace U9 with the new IC labeled "PRES 2.7". Make absolutely sure that the IC is installed right-side up (pin 1 at the upper left corner) and that all 24 pins have been seated into the socket.

Using an X-ACTO knife cut the U-shaped trace near U2. Make an opening in this trace at least as wide as the trace itself. This signals the presence of the modification to the Presetter software.

MAIN BOARD MODIFICATION

Set aside the Upper Assembly and retrieve the Lower Assembly. Remove the keyboard from the Lower Assembly by removing the four 8-32 screws which hold the keyboard to the bottom. Move the keyboard enough to gain access to U22; the keyboard cable need not be demated from J3.

Using a 24-pin IC removal tool pull out U22 from its socket.

Using a 24-pin IC insertion tool replace U22 with the new IC labeled "SYN 2.3K ". Make absolutely sure that the IC is installed right-side up (pin 1 at the upper left corner) and that all 24 pins have been seated into the socket.

REASSEMBLY Fig. 3.

Place the keyboard over the Lower Assembly and fasten with the four 8-32 screws removed earlier. Tighten firmly but not so tight that the screw heads distort the plastic (or rubber grommets, if present).

Position the Upper Assembly on its back directly behind the Lower Assembly.

Mate the 6-conductor power connector from the transformer to J6 on the Main Board, making absolutely sure it is connected properly. Damage will result from mismating this connector.

Mate the two 40-conductor ribbon cables to J2 and J4 on the Main Board, making sure they are not twisted.

Mate the three 10-conductor ribbon cables to J1, J5, and J7 on the Main Board, making sure that the triangle on each connector body lines up with the triangle on the mating connector body. (On J1 the triangle is on the back of the connector. On J5 and J7 the triangles are on the front.)

REASSEMBLY (Cont.)

Now close the Upper Assembly down over the Lower Assembly. As you do so, make sure the various ribbon cables do not interfere with the keyboard and are not caught between the case top and bottom. The case top will have to be positioned slightly forward in order to slip the forward edge under the keyboard. Lower the case top all the way until it seats against the bottom.

Fasten the top and bottom together with the ten 10-32 screws (8-32 for Clear models) removed earlier, tightening firmly but not so tight that the screw heads distort the plastic (or rubber grommets, if present).

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OPERATION OF THE INTERNAL PRESETTER CONTROLS

The internal Presetter controls are hidden behind heat vent #2 (second from the left as viewed from a normal playing position) and may be actuated with a key, toothpick or other implement. These three switches are, from left to right, STORE ENABLE, BANK, and RESET.

SET ALL CONTROLS TO MANUAL

1. Set RECALL switch to middle position
2. Momentarily actuate RESET

OVERLAY PRESETS 50-99 WITH FACTORY PRESETS

1. Position BANK switch to the left

Note: This does not erase user presets 50-99. They are available when BANK is positioned to right.

LOAD FACTORY PRESETS INTO 00-49 AND 50-99

1. Set RECALL to latched Recall position
2. Position STORE ENABLE to right
3. Position BANK to left
4. Press STORE pushbutton and hold
5. Turn on AC power. If power is already on, momentarily actuate RESET
6. After 1 second, release STORE pushbutton

Note: This operation will erase all user presets.

LOAD FACTORY PRESETS INTO 50-99 ONLY

Same as above except position STORE ENABLE to left. Note: This operation will erase user presets 50-99.

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LOAD FACTORY PRESETS INTO NON-VOLATILE MEMORY (FIGURE 5)

Occasionally it will be necessary to load the factory presets into non-volatile memory, usually after initial installation of the Presetter Module or replacement of the Lithium battery. This is done with the internal switches which are accessible through the heat-vent slot, second from the left as you view it from a normal playing position. Follow these steps in the order given:

1. Set the RECALL switch to latched RECALL.
2. Set internal switch #2 to the left ("factory" position).
3. Press the STORE pushbutton and hold.
4. Turn on the AC power switch. If the power is already on, momentarily actuate internal switch #3 by moving it to the left, then releasing.
5. Release the STORE pushbutton.
6. Set internal switch #2 to the right ("normal" position).

Verify the presence of presets in locations 00 through 99.

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3. Press the STORE pushbutton and hold.
4. Turn on the AC power switch. If the power is already on, momentarily actuate internal switch #3 by moving it to the left, then releasing.
5. Release the STORE pushbutton.
6. Set internal switch #2 to the right ("normal" position).

Verify the presence of presets in locations 00 through 99.

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SERVICE BULLETIN

SERIAL DATA INPUT MODIFICATION

Pentaphonic 8110 Series

I. DESCRIPTION

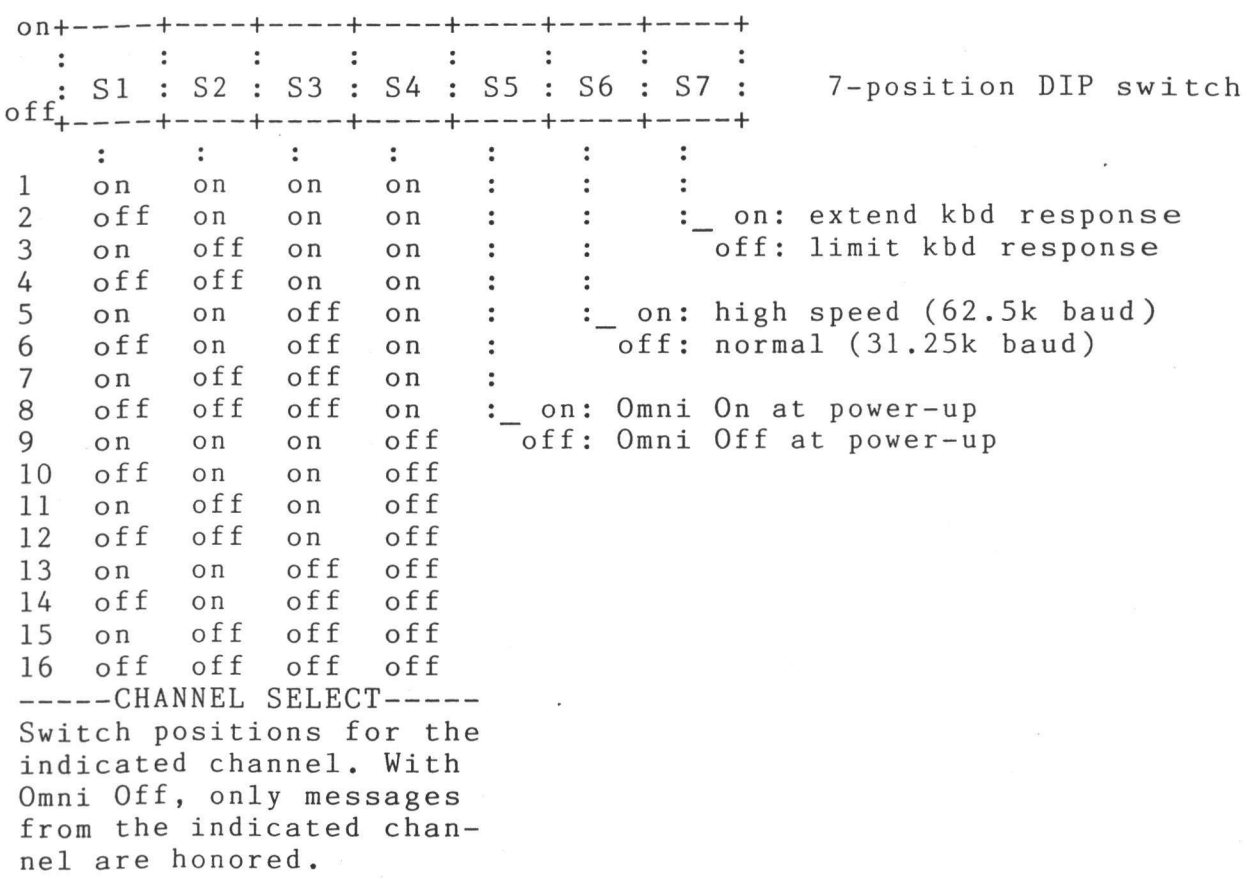
The 31100 interface modification allows the Pentaphonic synthesizer to accept MIDI-compatible serial data, which it converts to keyboard activity. The interface is receive-only and responds to note-on (1001nnnn 0kkkkkkk 01000000) and note-off (1000nnnn 0kkkkkkk 01000000) commands primarily. The only system commands it recognizes are All Notes Off (1011nnnn 01111011 00000000), Omni Off (1011nnnn 01111100 00000000), Omni On (1011nnnn 01111101 00000000), Reset (11111111), and Exclusive (11110000 00011010) which it interprets as interface self-test.

The modification consists of adding a wire to the Pentaphonic main board, drilling a number of holes in the case for the DIN connector, and attaching the 31100 circuit board and its associated cables.

The interface permits the Pentaphonic to receive in Mode 1 (Omni On Poly) or Mode 3 (Omni Off Poly). Since the serial data is applied to the Pentaphonic's keyboard circuit, anything which could be done from the keyboard manually will be available through the interface once the mod is installed. This includes Mono/Poly operation, oscillator detuning, sequencer programming, etc. Although it is possible to play the keyboard during serial input, it is not recommended as it will electrically stress the interface circuitry.

II. CONFIGURE THE INTERFACE

It is most convenient to configure the 31100 interface before installation, although it may be reconfigured any time. The 7-position DIP switch on the 31100 circuit board is used to select the Omni-off channel number, default channel mode, serial data rate, and Pentaphonic keyboard response, which when ON allows the Pentaphonic to respond to note messages outside its normal range by translating high-octave notes down and low-octave notes up by whole octave amounts. When OFF, note messages outside the Pentaphonic's range are ignored.



	S1	S2	S3	S4	S5	S6	S7
1	on	on	on	on			
2	off	on	on	on			
3	on	off	on	on			
4	off	off	on	on			
5	on	on	off	on			
6	off	on	off	on			
7	on	off	off	on			
8	off	off	off	on			
9	on	on	on	off			
10	off	on	on	off			
11	on	off	on	off			
12	off	off	on	off			
13	on	on	off	off			
14	off	on	off	off			
15	on	off	off	off			
16	off	off	off	off			

-----CHANNEL SELECT-----
Switch positions for the indicated channel. With Omni Off, only messages from the indicated channel are honored.

III. OPEN THE PENTAPHONIC

You will need at least a 24" X 30" area on your workbench or tabletop. Spread a clean terrycloth towel over the surface to protect the Pentaphonic case.

REQUIRED TOOLS

Large Philips screwdriver
Small Phillips screwdriver
Soldering iron
Electric drill
5/8" hole saw
7/64" drill bit

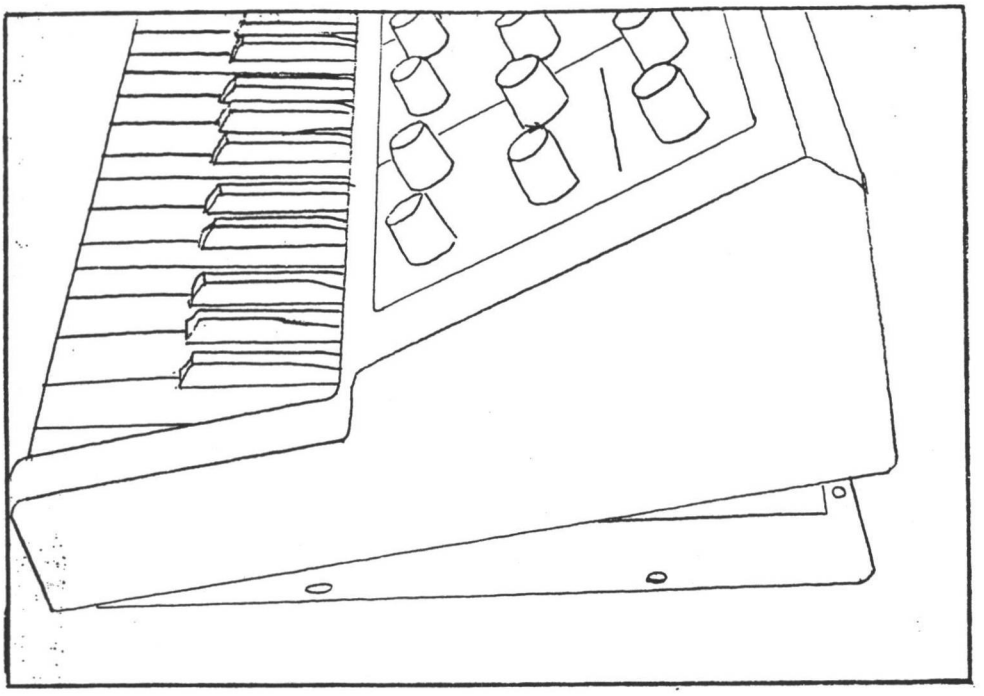
With the unit unplugged, open the Pentaphonic case by removing the ten 10-32 X 3/4 screws (8-32 in Clear models) from around the perimeter of the bottom cover. DO NOT at this time remove any of the seven 8-32 screws which are also on the bottom but located well inside the perimeter. (Fig. 1)

When all ten screws have been removed hold the top and bottom together to prevent their uncontrolled separation. Place the unit in the middle of the workspace in a normal playing position. Raise the back of the case a few inches, then slide it forward until the forward edge clears the keyboard. Raise the forward edge and lower the back until the upper assembly rests on its back.

Demate the two large 40-pin ribbon connectors at J2 and J4. Demate the 6-pin power connector J6 and the three 10-pin ribbon connectors J1, J5, and J7. If there are any additional cables installed between the upper and lower assemblies remove them at this time. Set aside the upper assembly temporarily.

Stand the lower assembly on the forward edge of the keyboard and remove the four 8-32 screws holding the keyboard to the lower assembly. Remove the keyboard and discard the old keyboard ribbon cable. Set aside the keyboard.

Remove the remaining three 8-32 screws which hold the main board to the case bottom.



Remove perimeter screws, raise back, slide forward

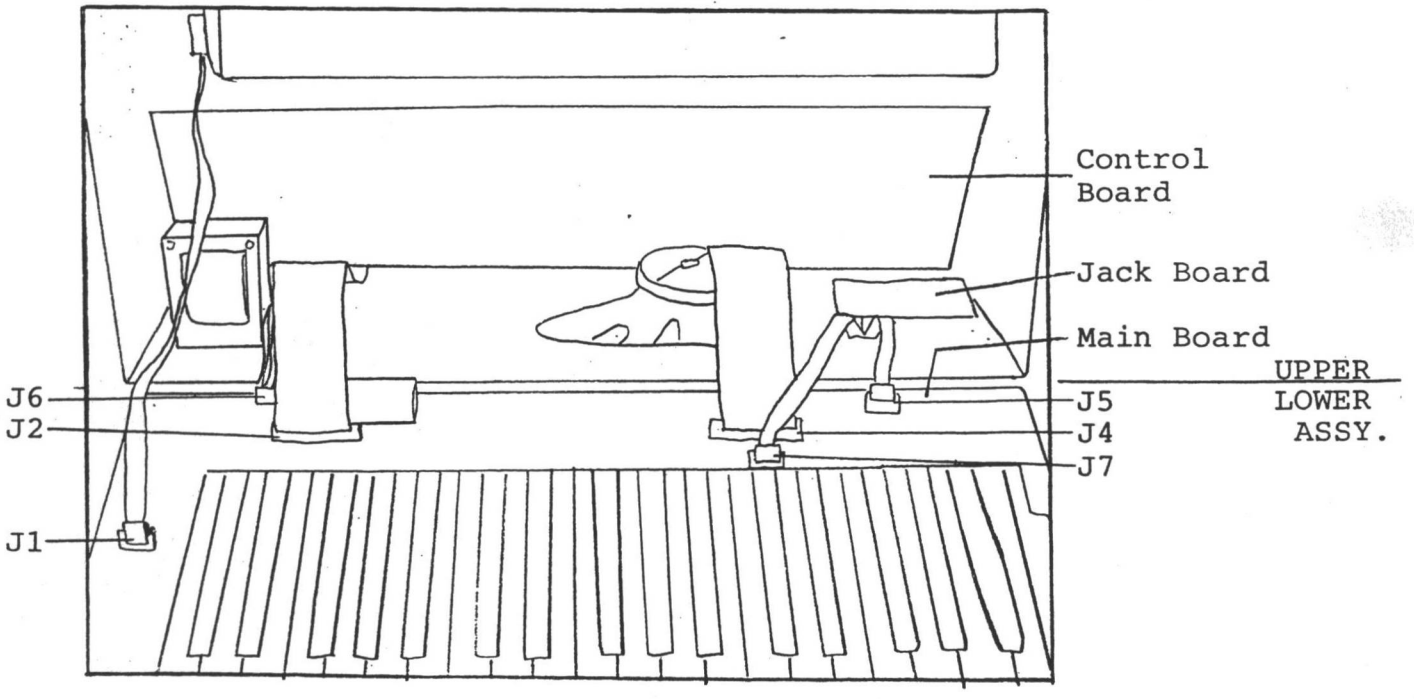


FIGURE 1

IV. INSTALL THE INTERFACE

Locate the 40-pin keyboard connector J3 from the bottom (foil side) of the main board. Carefully solder a 22 gauge wire from pin 1 of this connector to the 5 volt power trace. (Fig. 2A)

Reassemble the lower assembly. Position the main board on the case bottom and fasten using three 8-32 screws. Connect the new keyboard cable to J3, taking care to match triangles indicating pin 1. Connect the cable to the keyboard, then fasten the keyboard to the lower assembly with four 8-32 screws. Set aside the lower assembly.

Using the template provided, locate the holes for the DIN connector. This connector may be located on the back or right side of the instrument. Cut the 5/8" hole with a hole saw and drill the two 7/64" mounting holes. Fasten the DIN connector to the case using the 4-40 hardware provided.

Mate the DIN cable assembly to the 31100 circuit board as shown. Now remove the paper backing from the velcro pads on the bottom of the board and press firmly against the control board in the position shown. (Fig. 2B)

Installation of the mod is now complete.

V. CLOSE THE PENTAPHONIC

Position the upper assembly on its back directly behind the lower assembly. Mate the 6-conductor power cable to J6 on the main board, making absolutely sure it is connected properly. DAMAGE WILL RESULT FROM MISMATING THIS CONNECTOR. (Fig. 3)

Mate the two 40-conductor ribbon cables to J2 and J4 on the main board, making sure they are not twisted. Mate the three 10-conductor ribbon cables to J1, J5, and J7 on the main board, making sure that the triangles indicating pin 1 line up. Reconnect any other remaining cables including the new one at J1 of the 31100 board.

Now close the upper assembly down over the lower assembly. As you do so, make sure the various ribbon cables do not interfere with the keyboard and are not caught between the case top and bottom. The case top will have to be positioned slightly forward in order to slip its forward edge under the keyboard. Lower the case top all the way until it seats against the bottom.

Fasten the top and bottom together with ten 10-32 screws (8-32 for Clear models) removed earlier, tightening lightly so as not to distort the case or rubber grommets if present.

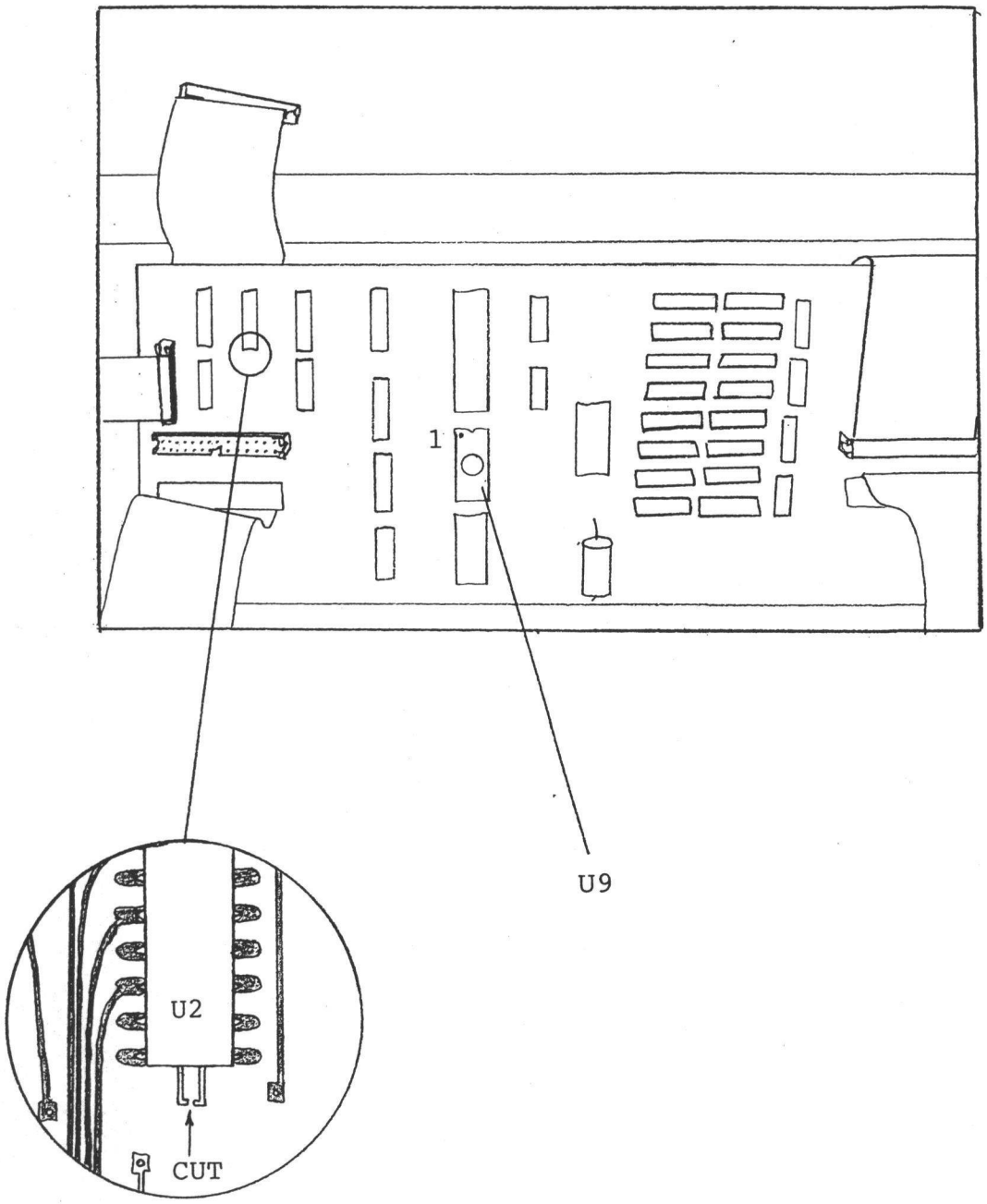
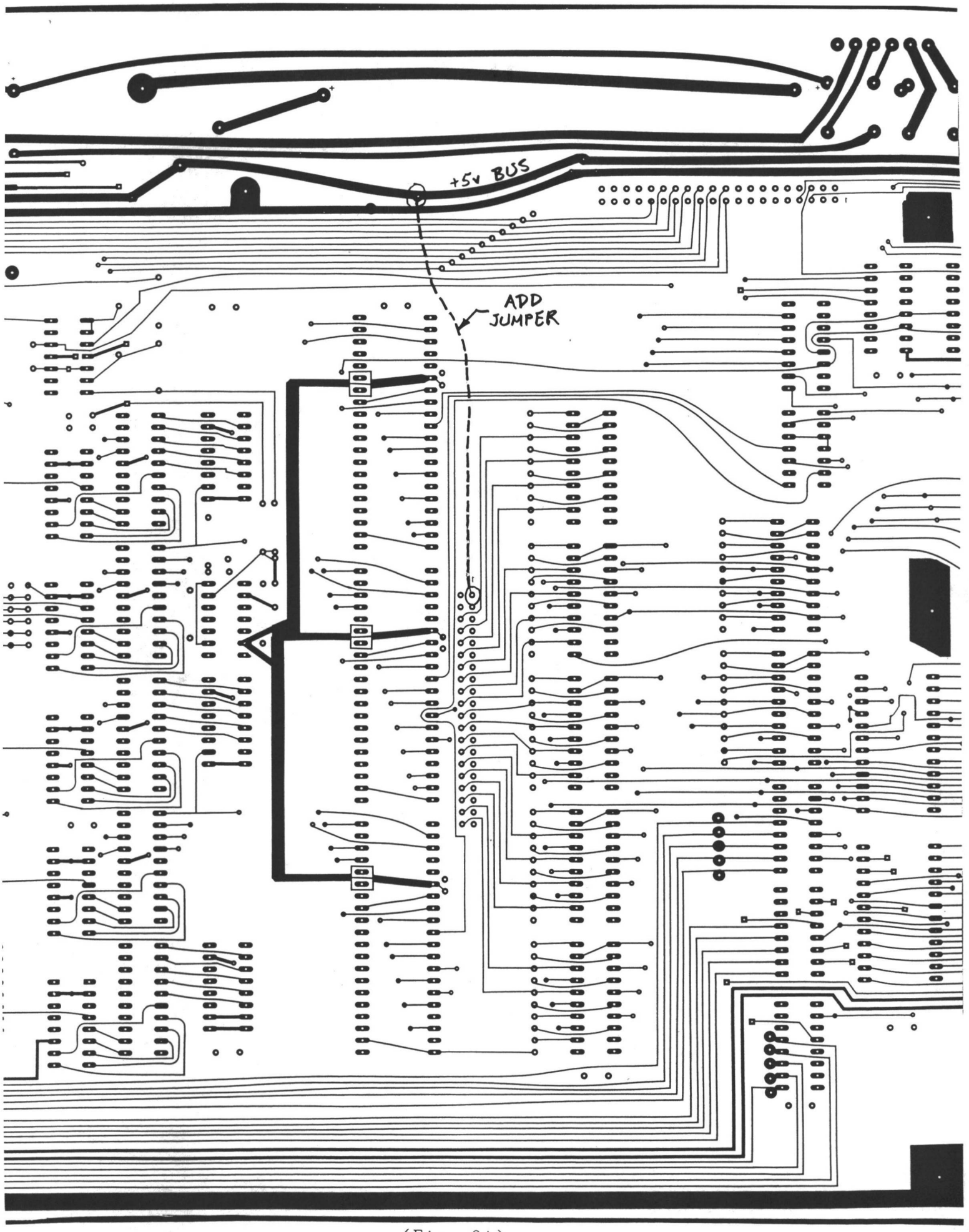
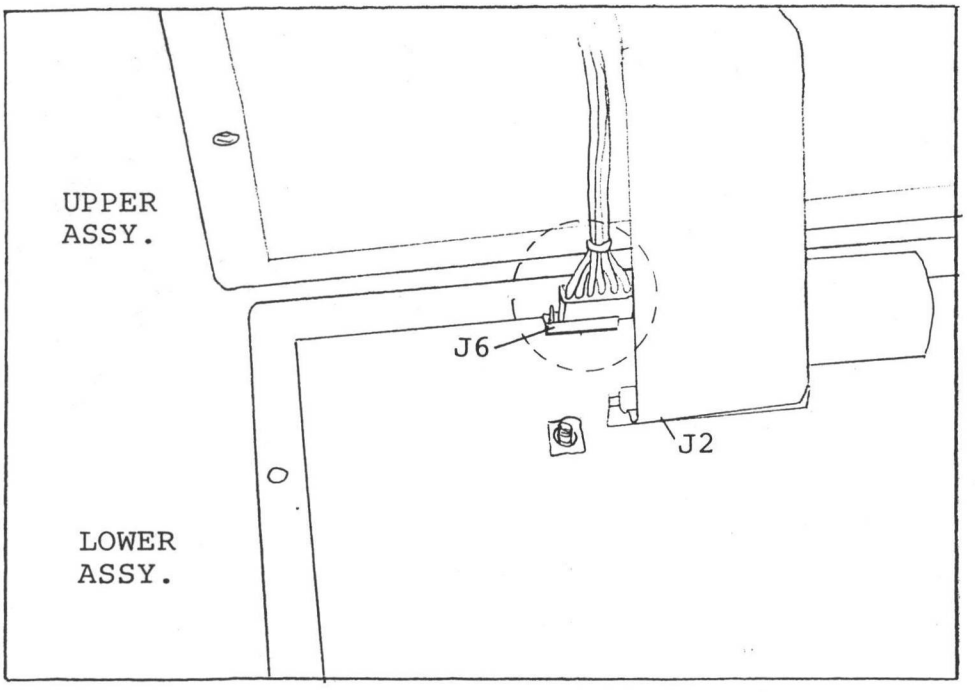


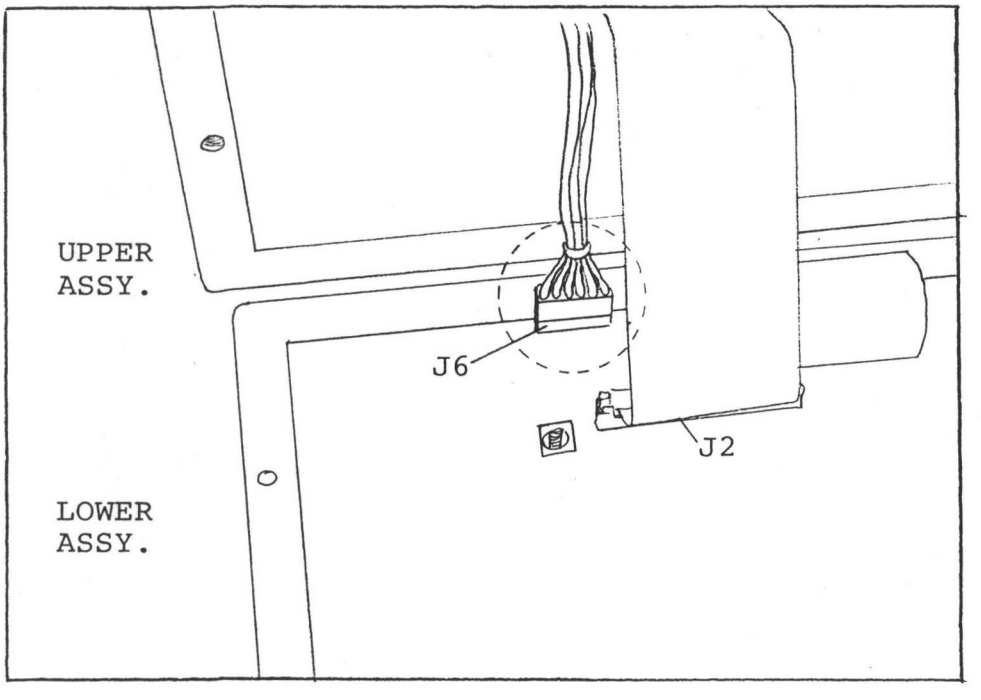
Fig. 2
PRESETTER BOARD MODIFICATION



(Fig. 2A)

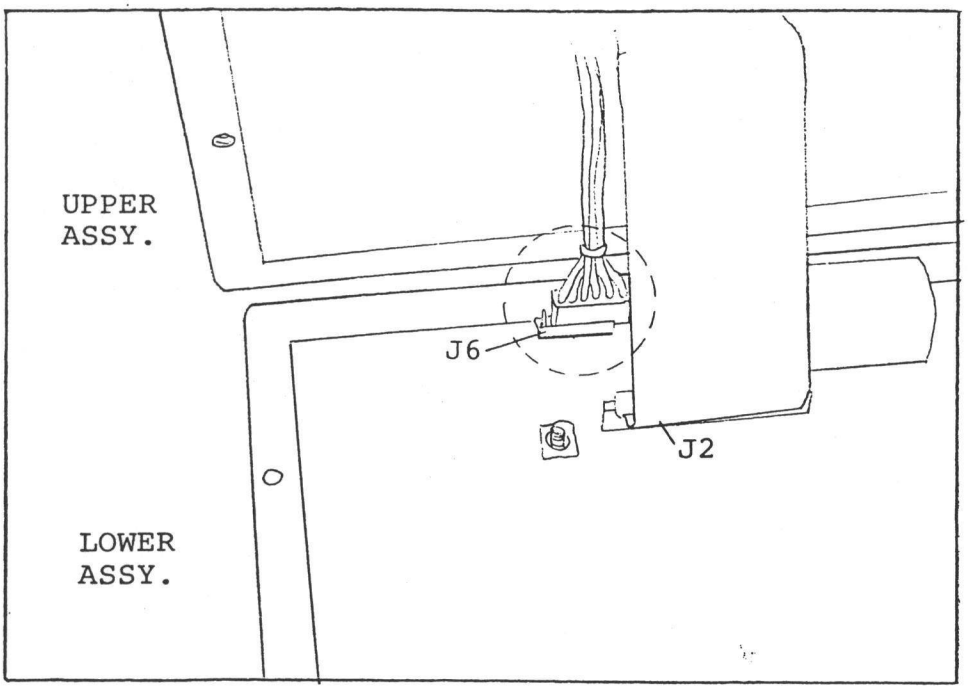


The WRONG way
to install J6

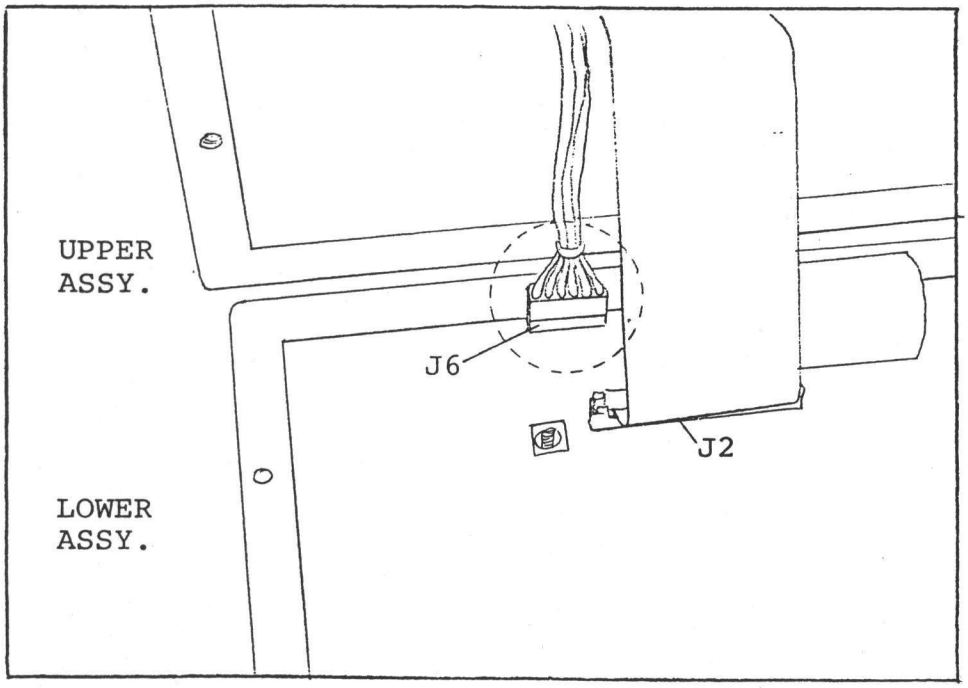


The right way
to install J6

FIGURE 3



The WRONG way
to install J6



The right way
to install J6

FIGURE 3

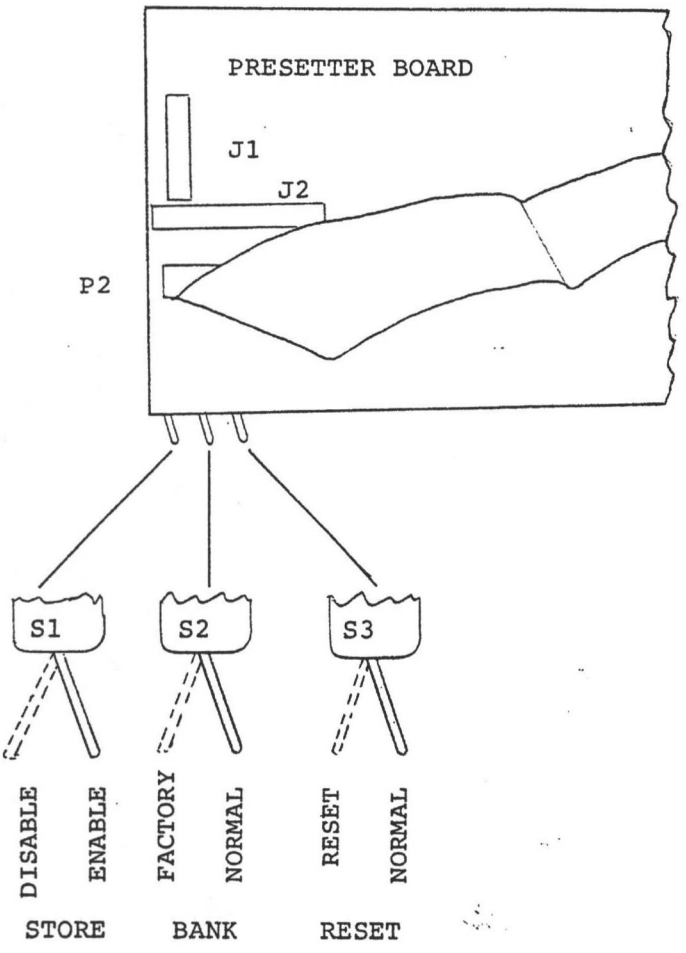

PRESETTER BOARD
J1
J2
P2
S1
S2
S3
DISABLE
ENABLE
FACTORY
NORMAL
RESET
NORMAL
STORE
BANK
RESET

FIGURE 5

GLEEMAN INSTRUMENT COMPANY
97 ELDORA DRIVE • MOUNTAIN VIEW, CALIFORNIA 94041

PHONE: 415 - 964 - 1464

SERVICE BULLETIN

VERIFY OPERATION

Position the RECALL switch to its middle (straight-up) position. Plug in the AC line cord and turn on the AC power switch. Verify that all front-panel control knobs and switches perform their function. Failure of any or all knobs to function properly could mean a mal-functioning Presetter Module.

Now set the leverswitch to '50' and set the RECALL switch to latched RECALL. The "Typical Piano" preset should be obtained. If it is not, it may mean that the Factory Presets are not loaded into non-volatile memory. See "Load Factory Presets into Non-volatile Memory". Verify the presence of presets in positions 00 through 99. Verify that you can store patches using the STORE pushbutton.

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SERVICE BULLETIN

VERIFY OPERATION

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CD Rom

1-5	Tuning Mod Ins	54	Holes
6	MIDI Instschematic	55	Sche
37	MIDI "PCB"	56	sche
8	Service Bulletin MIDI	57	upper assy
9-12	MIDI Install	58	letter
13-16	Preset Install	59	Sales letter
17-23	Tuning & Presetter	60	Load factory
24-29	Presetter install	61	verify op of presetter
-30	Software versions	62	switch pos
-31	Presetter test		
-32	Load presets		
-33	Switch positions		
34	Parts list		
-35	Sche		
36	Parts		
-37	Sche		
-38	Control Bd assy		
-39	Main Bd assy		
-40	Sche		
-41	"		
-42	" Presetter		
43	Parts		
44	Holes drilling Main		
45	Schem control bd		
46	schem main		
47	Lower Assy		
48-58	Drum interface instal		

415-988-8628

SYN 2.2L — F-boards only, no BBU, osc detuning 600-note seq
SYN 2.3K — G-boards only, no BBU, osc detuning
DENTON — F-board, no BBU, osc detuning, instant glide
no seq delay
SYN2.3H — G-board, "Chris Page Special"
SYN2.2K1 — F-board, no BBU
SYN2.2 K2 — F-board, BBU
SYN2.2K4 — F-board, no BBU, 300-note seq
SYN2.3K5 - G-board, noBBU, chorus-off mod
SYN2.3K6 - G-board, BBU, chorus-off mod
SYN 2.2L1 - F-board, no BBU, instant glide mod
SYN 2.2L2 - F-board, BBU, instant glide
SYN 2.2L3 - F-board, no BBU, 300-note seq, instant glide mod
SYN 2.3L4 - G-board, no BBU, chorus off mod, instant glide mod
SYN 2.3L5 - G-board, BBU, chorus off mod, instant glide mod

Table 6. Instruction Set Summary (Continued)

Mnemonic	Instruction Code D_7 D_6 D_5 D_4 D_3 D_2 D_1 D_0	Operations Description
RETURN (Continued)		
RNZ	1 1 0 0 0 0 0 0	Return on no zero
RP	1 1 1 1 0 0 0 0	Return on positive
RM	1 1 1 1 1 0 0 0	Return on minus
RPE	1 1 1 0 1 0 0 0	Return on parity even
RPO	1 1 1 0 0 0 0 0	Return on parity odd
RESTART		
RST	1 1 A A A 1 1 1	Restart
INPUT/OUTPUT		
IN	1 1 0 1 1 0 1 1	Input
OUT	1 1 0 1 0 0 1 1	Output
INCREMENT AND DECREMENT		
INR r	0 0 D D D 1 0 0	Increment register
DCR r	0 0 D D D 1 0 1	Decrement register
INR M	0 0 1 1 0 1 0 0	Increment memory
DCR M	0 0 1 1 0 1 0 1	Decrement memory
INX B	0 0 0 0 0 0 1 1	Increment B & C registers
INX D	0 0 0 1 0 0 1 1	Increment D & E registers
INX H	0 0 1 0 0 0 1 1	Increment H & L registers
DCX B	0 0 0 0 1 0 1 1	Decrement B & C
DCX D	0 0 0 1 1 0 1 1	Decrement D & E
DCX H	0 0 1 0 1 0 1 1	Decrement H & L
ADD		
ADD r	1 0 0 0 0 S S S	Add register to A
ADC r	1 0 0 0 1 S S S	Add register to A with carry
ADD M	1 0 C 0 0 1 1 0	Add memory to A
ADC M	1 0 0 0 1 1 1 0	Add memory to A with carry
ADI	1 1 0 0 0 1 1 0	Add immediate to A
ACI	1 1 0 0 1 1 1 0	Add immediate to A with carry
DAD B	0 0 0 0 1 0 0 1	Add B & C to H & L
ADD (Continued)		
DAD D	0 0 0 1 1 0 0 1	Add D & E to H & L
DAD H	0 0 1 0 1 0 0 1	Add H & L to H & L
DAD SP	0 0 1 1 1 0 0 1	Add stack pointer to H & L
SUBTRACT		
SUB r	1 0 0 1 0 S S S	Subtract register from A
SBB r	1 0 0 1 1 S S S	Subtract register from A with borrow
SUB M	1 0 0 1 0 1 1 0	Subtract memory from A
SBB M	1 0 0 1 1 1 1 0	Subtract memory from A with borrow
SUI	1 1 0 1 0 1 1 0	Subtract immediate from A
SBI	1 1 0 1 1 1 1 0	Subtract immediate from A with borrow
LOGICAL		
ANA r	1 0 1 0 0 S S S	And register with A
XRA r	1 0 1 0 1 S S S	Exclusive OR register with A
ORA r	1 0 1 1 0 S S S	OR register with A
CMP r	1 0 1 1 1 S S S	Compare register with A
ANA M	1 0 1 0 0 1 1 0	And memory with A
XRA M	1 0 1 0 1 1 1 0	Exclusive OR memory with A
ORA M	1 0 1 1 0 1 1 0	OR memory with A
CMP M	1 0 1 1 1 1 1 0	Compare memory with A
ANI	1 1 1 0 0 1 1 0	And immediate with A
XRI	1 1 1 0 1 1 1 0	Exclusive OR immediate with A
ORI	1 1 1 1 0 1 1 0	OR immediate with A
CPI	1 1 1 1 1 1 1 0	Compare immediate with A

Table 6. Instruction Set Summary (Continued)

Mnemonic	Instruction Code D_7 D_6 D_5 D_4 D_3 D_2 D_1 D_0	Operations Description
ROTATE		
RLC	0 0 0 0 0 1 1 1	Rotate A left
RRC	0 0 0 0 1 1 1 1	Rotate A right
RAL	0 0 0 1 0 1 1 1	Rotate A left through carry
RAR	0 0 0 1 1 1 1 1	Rotate A right through carry
SPECIALS		
CMA	0 0 1 0 1 1 1 1	Complement A
STC	0 0 1 1 0 1 1 1	Set carry
CMC	0 0 1 1 1 1 1 1	Complement carry
DAA	0 0 1 0 0 1 1 1	Decimal adjust A

Mnemonic	Instruction Code D_7 D_6 D_5 D_4 D_3 D_2 D_1 D_0	Operations Description
CONTROL		
EI	1 1 1 1 1 0 1 1	Enable Interrupts
DI	1 1 1 1 0 0 1 1	Disable Interrupt
NOP	0 0 0 0 0 0 0 0	No-operation
HLT	0 1 1 1 0 1 1 0	Halt
NEW 8085AH INSTRUCTIONS		
RIM	0 0 1 0 0 0 0 0	Read Interrupt Mask
SIM	0 0 1 1 0 0 0 0	Set Interrupt Mask

NOTES:
1. DDS or SSS: B 000, C 001, D 010, E011, H 100, L101, Memory 110, A 111.
2. Two possible cycle times (6/12) indicate instruction cycles dependent on condition flags.

8085AH/8085AH-2/8085AH-1
8-BIT HMOS MICROPROCESSORS

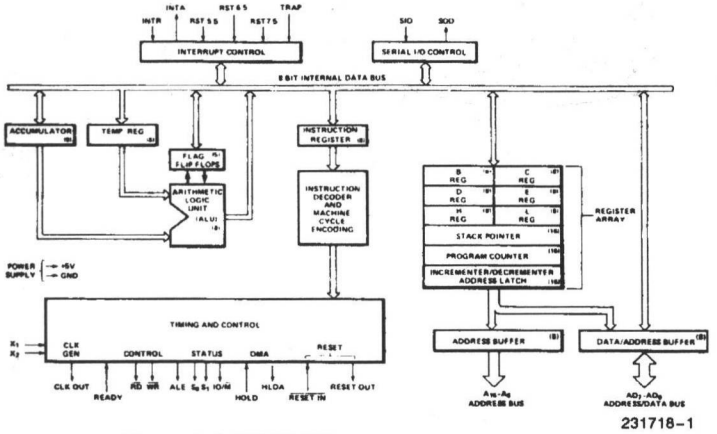
- **Single +5V Power Supply with 10% Voltage Margins**
- **3 MHz, 5 MHz and 6 MHz Selections Available**
- **20% Lower Power Consumption than 8085A for 3 MHz and 5 MHz**
- **1.3 μs Instruction Cycle (8085AH); 0.8 μs (8085AH-2); 0.67 μs (8085AH-1)**
- **100% Software Compatible with 8080A**
- **On-Chip Clock Generator (with External Crystal, LC or RC Network)**
- **On-Chip System Controller; Advanced Cycle Status Information Available for Large System Control**
- **Four Vectored Interrupt Inputs (One is Non-Maskable) Plus an 8080A-Compatible Interrupt**
- **Serial In/Serial Out Port**
- **Decimal, Binary and Double Precision Arithmetic**
- **Direct Addressing Capability to 64K Bytes of Memory**
- **Available in 40-Lead Cerdip and Plastic Packages**
  (See Packaging Spec., Order #231369)

1

The Intel 8085AH is a complete 8-bit parallel Central Processing Unit (CPU) implemented in N-channel, depletion load, silicon gate technology (HMOS). Its instruction set is 100% software compatible with the 8080A microprocessor, and it is designed to improve the present 8080A's performance by higher system speed. Its high level of system integration allows a minimum system of three IC's [8085AH (CPU), 8156H (RAM/IO) and 8755A (EPROM/IO)] while maintaining total system expandability. The 8085AH-2 and 8085AH-1 are faster versions of the 8085AH.

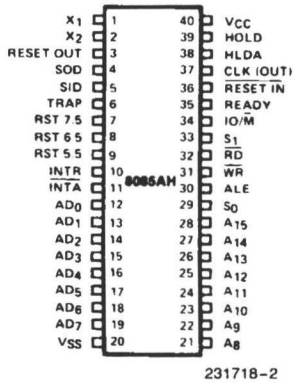
The 8085AH incorporates all of the features that the 8224 (clock generator) and 8228 (system controller) provided for the 8080A, thereby offering a higher level of system integration.

The 8085AH uses a multiplexed data bus. The address is split between the 8-bit address bus and the 8-bit data bus. The on-chip address latches of 8155H/8156H/8755A memory products allow a direct interface with the 8085AH.



231718-1

Figure 1. 8085AH CPU Functional Block Diagram



231718-2

Figure 2. 8085AH Pin Configuration

Table 1. Pin Description

Symbol	Type	Name and Function
A_8–A_{15}	O	**ADDRESS BUS:** The most significant 8 bits of memory address or the 8 bits of the I/O address, 3-stated during Hold and Halt modes and during RESET.
AD_{0-7}	I/O	**MULTIPLEXED ADDRESS/DATA BUS:** Lower 8 bits of the memory address (or I/O address) appear on the bus during the first clock cycle (T state) of a machine cycle. It then becomes the data bus during the second and third clock cycles.
ALE	O	**ADDRESS LATCH ENABLE:** It occurs during the first clock state of a machine cycle and enables the address to get latched into the on-chip latch of peripherals. The falling edge of ALE is set to guarantee setup and hold times for the address information. The falling edge of ALE can also be used to strobe the status information. ALE is never 3-stated.
S_0, S_1 and IO/$\overline{M}$	O	**MACHINE CYCLE STATUS:** **IO/$\overline{M}$ S_1 S_0 Status** 0 0 1 Memory write 0 1 0 Memory read 1 0 1 I/O write 1 1 0 I/O read 0 1 1 Opcode fetch 1 1 1 Interrupt Acknowledge * 0 0 Halt * X X Hold * X X Reset * = 3-state (high impedance) X = unspecified S_1 can be used as an advanced R/$\overline{W}$ status. IO/$\overline{M}$, S_0 and S_1 become valid at the beginning of a machine cycle and remain stable throughout the cycle. The falling edge of ALE may be used to latch the state of these lines.
$\overline{RD}$	O	**READ CONTROL:** A low level on $\overline{RD}$ indicates the selected memory or I/O device is to be read and that the Data Bus is available for the data transfer, 3-stated during Hold and Halt modes and during RESET.
$\overline{WR}$	O	**WROTE CONTROL:** A low level on $\overline{WR}$ indicates the data on the Data Bus is to be written into the selected memory or I/O location. Data is set up at the trailing edge of $\overline{WR}$. 3-stated during Hold and Halt modes and during RESET.
READY	I	**READY:** If READY is high during a read or write cycle, it indicates that the memory or peripheral is ready to send or receive data. If READY is low, the CPU will wait an integral number of clock cycles for READY to go high before completing the read or write cycle. READY must conform to specified setup and hold times.
HOLD	I	**HOLD:** Indicates that another master is requesting the use of the address and data buses. The CPU, upon receiving the hold request, will relinquish the use of the bus as soon as the completion of the current bus transfer. Internal processing can continue. The processor can regain the bus only after the HOLD is removed. When the HOLD is acknowledged, the Address, Data $\overline{RD}$, $\overline{WR}$, and IO/$\overline{M}$ lines are 3-stated.
HLDA	O	**HOLD ACKNOWLEDGE:** Indicates that the CPU has received the HOLD request and that it will relinquish the bus in the next clock cycle. HILDA goes low after the Hold request is removed. The CPU takes the bus one half clock cycle after HLDA goes low.
INTR	I	**INTERRUPT REQUEST:** Is used as a general purpose interrupt. It is sampled only during the next to the last clock cycle of an instruction and during Hold and Halt states. If it is active, the Program Counter (PC) will be inhibited from incrementing and an $\overline{INTA}$ will be issued. During this cycle a RESTART or CALL instruction can be inserted to jump to the interrupt service routine. The INTR is enabled and disabled by software. It is disabled by Reset and immediately after an interrupt is accepted.

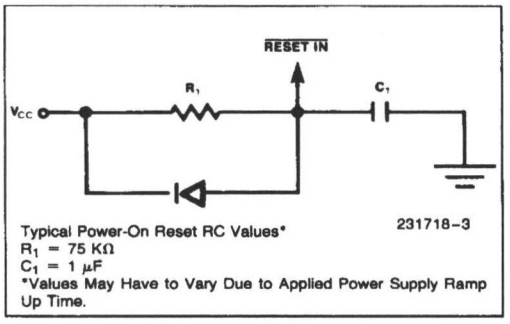
Table 1. Pin Description (Continued)

Symbol	Type	Name and Function
$\overline{INTA}$	O	**INTERRUPT ACKNOWLEDGE:** Is used instead of (and has the same timing as) $\overline{RD}$ during the Instruction cycle after an INTR is accepted. It can be used to activate an 8259A Interrupt chip or some other interrupt port.
RST 5.5 RST 6.5 RST 7.5	I	**RESTART INTERRUPTS:** These three inputs have the same timing as INTR except they cause an internal RESTART to be automatically inserted. The priority of these interrupt is ordered as shown in Table 2. These interrupts have a higher priority than INTR. In addition, they may be individually masked out using the SIM instruction.
TRAP	I	**TRAP:** Trap interrupt is a non-maskable RESTART interrupt. It is recognized at the same time as INTR or RST 5.5–7.5. It is unaffected by any mask or Interrupt Enable. It has the highest priority of any interrupt. (See Table 2.)
$\overline{RESET\ IN}$	I	**RESET IN:** Sets the Program Counter to zero and resets the Interrupt Enable and HLDA flip-flops. The data and address buses and the control lines are 3-stated during RESET and because of the asynchronous nature of RESET, the processor's internal registers and flags may be altered by RESET with unpredictable results. $\overline{RESET\ IN}$ is a Schmitt-triggered input, allowing connection to an R-C network for power-on RESET delay (see Figure 3). Upon power-up, $\overline{RESET\ IN}$ must remain low for at least 10 ms after minimum V_{CC} has been reached. For proper reset operation after the power-up duration, $\overline{RESET\ IN}$ should be kept low a minimum of three clock periods. The CPU is held in the reset condition as long as $\overline{RESET\ IN}$ is applied.
RESET OUT	O	**RESET OUT:** Reset Out indicates CPU is being reset. Can be used as a system reset. The signal is synchronized to the processor clock and lasts an integral number of clock periods.
X_1, X_2	I	**X_1 and X_2:** Are connected to a crystal, LC, or RC network to drive the internal clock generator. X_1 can also be an external clock input from a logic gate. The input frequency is divided by 2 to give the processor's internal operating frequency.
CLK	O	**CLOCK:** Clock output for use as a system clock. The period of CLK is twice the X_1, X_2 input period.
SID	I	**SERIAL INPUT DATA LINE:** The data on this line is loaded into accumulator bit 7 whenever a RIM instruction is executed.
SOD	O	**SERIAL OUTPUT DATA LINE:** The output SOD is set or reset as specified by the SIM instruction.
V_{CC}		**POWER:** +5 volt supply.
V_{SS}		**GROUND:** Reference.

Table 2. Interrupt Priority, Restart Address and Sensitivity

Name	Priority	Address Branched to(1) When Interrupt Occurs	Type Trigger
TRAP	1	24H	Rising Edge AND High Level until Sampled
RST 7.5	2	3CH	Rising Edge (Latched)
RST 6.5	3	34H	High Level until Sampled
RST 5.5	4	2CH	High Level until Sampled
INTR	5	(Note 2)	High Level until Sampled

NOTES:
1. The processor pushes the PC on the stack before branching to the indicated address.
2. The address branched to depends on the instruction provided to the CPU when the interrupt is acknowledged.



Typical Power-On Reset RC Values*
R_1 = 75 KΩ
C_1 = 1 μF
*Values May Have to Vary Due to Applied Power Supply Ramp Up Time.

Figure 3. Power-On Reset Circuit

FUNCTIONAL DESCRIPTION

The 8085AH is a complete 8-bit parallel central processor. It is designed with N-channel, depletion load, silicon gate technology (HMOS), and requires a single +5V supply. Its basic clock speed is 3 MHz (8085AH), 5 MHz (8085AH-2), or 6 MHz (8085-AH-1), thus improving on the present 8080A's performance with higher system speed. Also it is designed to fit into a minimum system of three IC's: The CPU (8085AH), a RAM/IO (8156H), and an EPROM/IO chip (8755A).

The 8085AH has twelve addressable 8-bit registers. Four of them can function only as two 16-bit register pairs. Six others can be used interchangeably as 8-bit registers or as 16-bit register pairs. The 8085AH register set is as follows:

Mnemonic	Register	Contents
ACC or A	Accumulator	8 Bits
PC	Program Counter	16-Bit Address
BC, DE, HL	General-Purpose Registers; data pointer (HL)	8-Bits x 6 or 16 Bits x 3
SP	Stack Pointer	16-Bit Address
Flags or F	Flag Register	5 Flags (8-Bit Space)

The 8085AH uses a multiplexed Data Bus. The address is split between the higher 8-bit Address Bus and the lower 8-bit Address/Data Bus. During the first T state (clock cycle) of a machine cycle the low order address is sent out on the Address/Data bus. These lower 8 bits may be latched externally by the Address Latch Enable signal (ALE). During the rest of the machine cycle the data bus is used for memory or I/O data.

The 8085AH provides $\overline{RD}$, $\overline{WR}$, S_0, S_1, and IO/$\overline{M}$ signals for bus control. An Interrupt Acknowledge signal ($\overline{INTA}$) is also provided. HOLD and all Interrupts are synchronized with the processor's internal clock. The 8085AH also provides Serial Input Data (SID) and Serial Output Data (SOD) lines for simple serial interface.

In addition to these features, the 8085AH has three maskable, vector interrupt pins, one nonmaskable TRAP interrupt, and a bus vectored interrupt, INTR.

INTERRUPT AND SERIAL I/O

The 8085AH has 5 interrupt inputs: INTR, RST 5.5, RST 6.5, RST 7.5, and TRAP. INTR is identical in function to the 8080A INT. Each of the three RESTART inputs, 5.5, 6.5, and 7.5, has a programmable mask. TRAP is also a RESTART interrupt but it is nonmaskable.

The three maskable interrupt cause the internal execution of RESTART (saving the program counter in the stack and branching to the RESTART address) if the interrupts are enabled and if the interrupt mask is not set. The nonmaskable TRAP causes the internal execution of a RESTART vector independent of the state of the interrupt enable or masks. (See Table 2.)

There are two different types of inputs in the restart interrupts. RST 5.5 and RST 6.5 are *high level-sensitive* like INTR (and INT on the 8080) and are recognized with the same timing as INTR. RST 7.5 is *rising edge-sensitive.*

For RST 7.5, only a pulse is required to set an internal flip-flop which generates the internal interrupt request (a normally high level signal with a low going pulse is recommended for highest system noise immunity). The RST 7.5 request flip-flop remains set until the request is serviced. Then it is reset automatically. This flip-flop may also be reset by using the SIM instruction or by issuing a $\overline{RESET\ IN}$ to the 8085AH. The RST 7.5 internal flip-flop will be set by a pulse on the RST 7.5 pin even when the RST 7.5 interrupt is masked out.

The status of the three RST interrupt masks can only be affected by the SIM instruction and $\overline{RESET\ IN}$. (See SIM, Chapter 5 of the 8080/8085 User's Manual.)

The interrupts are arranged in a fixed priority that determines which interrupt is to be recognized if more than one is pending as follows: TRAP—highest priority, RST 7.5, RST 6.5, RST 5.5, INTR—lowest priority. This priority scheme does not take into account the priority of a routine that was started by a higher priority interrupt. RST 5.5 can interrupt an RST 7.5 routine if the interrupts are re-enabled before the end of the RST 7.5 routine.

The TRAP interrupt is useful for catastrophic events such as power failure or bus error. The TRAP input is recognized just as any other interrupt but has the

highest priority. It is not affected by any flag or mask. The TRAP input is both *edge and level sensitive.* The TRAP input must go high and remain high until it is acknowledged. It will not be recognized again until it goes low, then high again. This avoids any false triggering due to noise or logic glitches. Figure 4 illustrates the TRAP interrupt request circuitry within the 8085AH. Note that the servicing of any interrupt (TRAP, RST 7.5, RST 6.5, RST 5.5, INTR) disables all future interrupts (except TRAPs) until an EI instruction is executed.

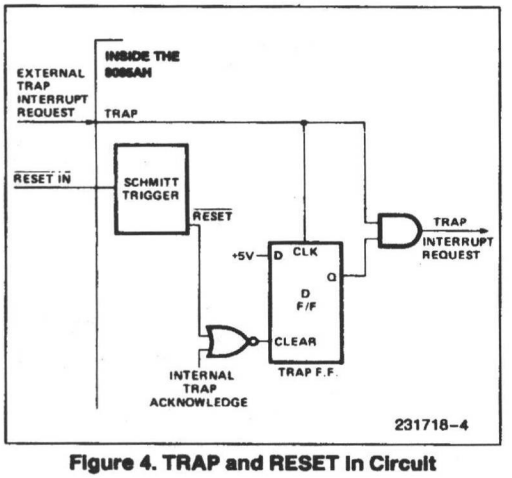


Figure 4. TRAP and RESET In Circuit

The TRAP interrupt is special in that it disables interrupts, but preserves the previous interrupt enable status. Performing the first RIM instruction following a TRAP interrupt allows you to determine whether interrupts were enabled or disabled prior to the TRAP. All subsequent RIM instructions provide current interrupt enable status. Performing a RIM instruction following INTR, or RST 5.5–7.5 will provide current Interrupt Enable status, revealing that interrupts are disabled. See the description of the RIM instruction in the 8080/8085 Family User's Manual.

The serial I/O system is also controlled by the RIM and SIM instruction. SID is read by RIM, and SIM sets the SOD data.

DRIVING THE X_1 AND X_2 INPUTS

You may drive the clock inputs of the 8085AH, 8085AH-2, or 8085AH-1 with a crystal, an LC tuned circuit, an RC network, or an external clock source. The crystal frequency must be at least 1 MHz, and must be twice the desired internal clock frequency; hence, the 8085AH is operated with a 6 MHz crystal (for 3 MHz clock), the 8085AH-2 operated with a 10 MHz crystal (for 5 MHz clock), and the 8085AH-1 can be operated with a 12 MHz crystal (for 6 MHz clock). If a crystal is used, it must have the following characteristics:

Parallel resonance at twice the clock frequency desired
C_L (load capacitance) $\leq$ 30 pF
C_S (Shunt capacitance) $\leq$ 7 pF
R_S (equivalent shunt resistance) $\leq 75\Omega$
Drive level: 10 mW
Frequency tolerance: $\pm 0.005\%$ (suggested)

Note the use of the 20 pF capacitor between X_2 and ground. This capacitor is required with crystal frequencies below 4 MHz to assure oscillator startup at the correct frequency. A parallel-resonant LC citcuit may be used as the frequency-determining network for the 8085AH, providing that its frequency tolerance of approximately $\pm 10\%$ is acceptable. The components are chosen from the formula:

$$f = \frac{1}{2\pi\sqrt{L(C_{ext} + C_{int})}}$$

To minimize variations in frequency, it is recommended that you choose a value for C_{ext} that is at least twice that of C_{int}, or 30 pF. The use of an LC circuit is not recommended for frequencies higher than approximately 5 MHz.

An RC circuit may be used as the frequency-determining network for the 8085AH if maintaining a precise clock frequency is of no importance. Variations in the on-chip timing generation can cause a wide variation in frequency when using the RC mode. Its advantage is its low component cost. The driving frequency generated by the circuit shown is approximately 3 MHz. It is not recommended that frequencies greatly higher or lower than this be attempted.

Figure 5 shows the recommended clock driver circuits. Note in d and e that pullup resistors are required to assure that the high level voltage of the input is at least 4V and maximum low level voltage of 0.8V.

For driving frequencies up to and including 6 MHz you may supply the driving signal to X_1 and leave X_2 open-circuited (Figure 5d). If the driving frequency is from 6 MHz to 12 MHz, stability of the clock generator will be improved by driving both X_1 and X_2 with a push-pull source (Figure 5e). To prevent self-oscillation of the 8085AH, be sure that X_2 is not coupled back to X_1 through the driving circuit.

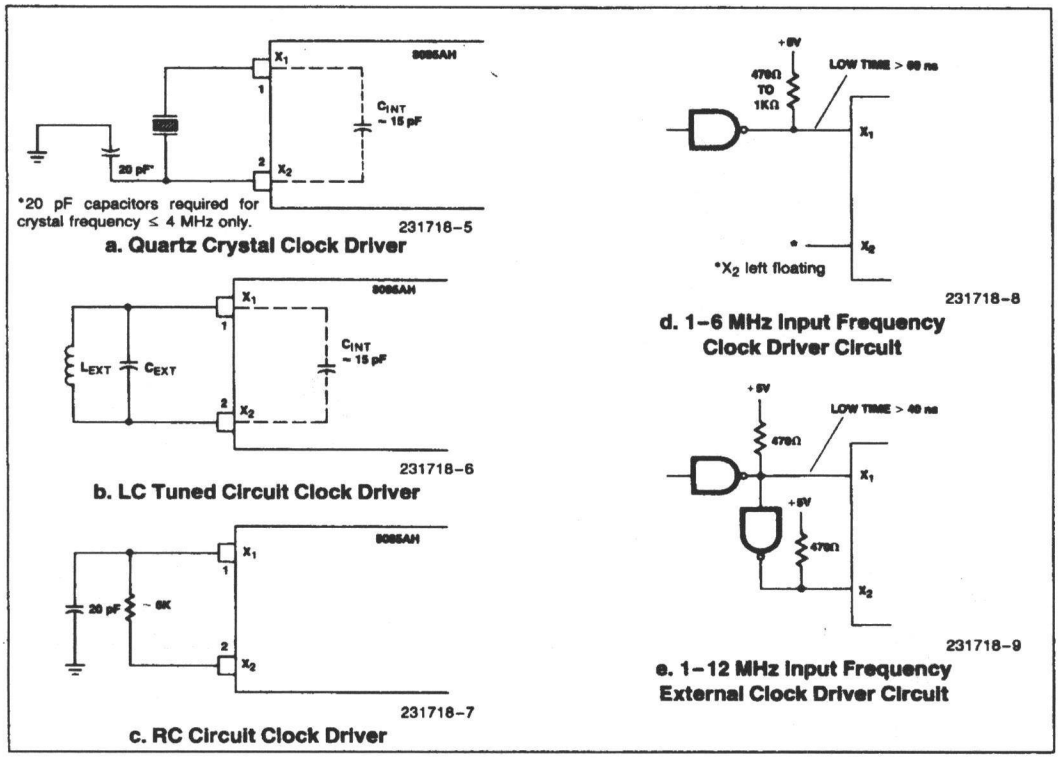


Figure 5. Clock Driver Circuits

GENERATING AN 8085AH WAIT STATE

If your system requirements are such that slow memories or peripheral devices are being used, the circuit shown in Figure 6 may be used to insert one WAIT state in each 8085AH machine cycle.

The D flip-flops should be chosen so that
- CLK is rising edge-triggered
- CLEAR is low-level active.

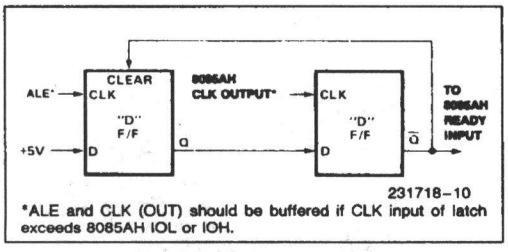


Figure 6. Generation of a Wait State for 8085AH CPU

As in the 8080, the READY line is used to extend the read and write pulse lengths so that the 8085AH can be used with slow memory. HOLD causes the CPU to relinquish the bus when it is through with it by floating the Address and Data Buses.

SYSTEM INTERFACE

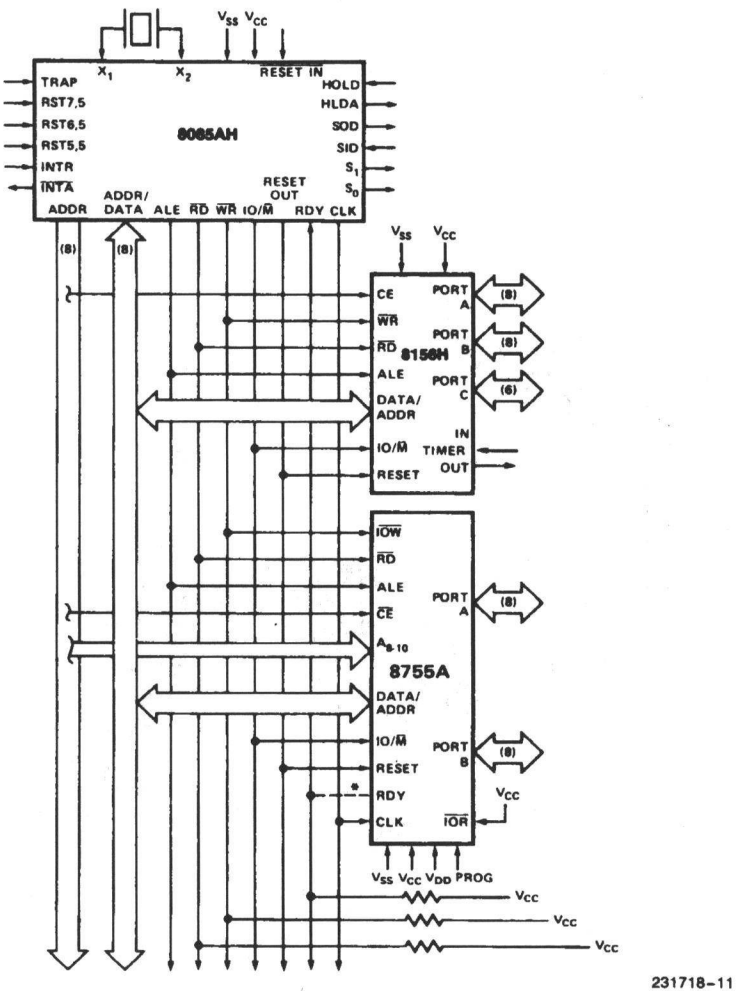
The 8085AH family includes memory components, which are directly compatible to the 8085AH CPU. For example, a system consisting of the three chips, 8085AH, 8156H and 8755A will have the following features:

- 2K Bytes EPROM
- 256 Bytes RAM
- 1 Timer/Counter
- 4 8-bit I/O Ports
- 1 6-bit I/O Port
- 4 Interrupt Levels
- Serial In/Serial Out Ports

This minimum system, using the standard I/O technique is as shown in Figure 7.

In addition to the standard I/O, the memory mapped I/O offers an efficient I/O addressing technique. With this technique, an area of memory address space is assigned for I/O address, thereby, using the memory address for I/O manipulation. Figure 8 shows the system configuration of Memory Mapped I/O using 8085AH.

The 8085AH CPU can also interface with the standard memory that does *not* have the multiplexed address/data bus. It will require a simple 8-bit latch as shown in Figure 9.



*NOTE:
Optional Connection

Figure 7. 8085AH Minimum System (Standard I/O Technique)

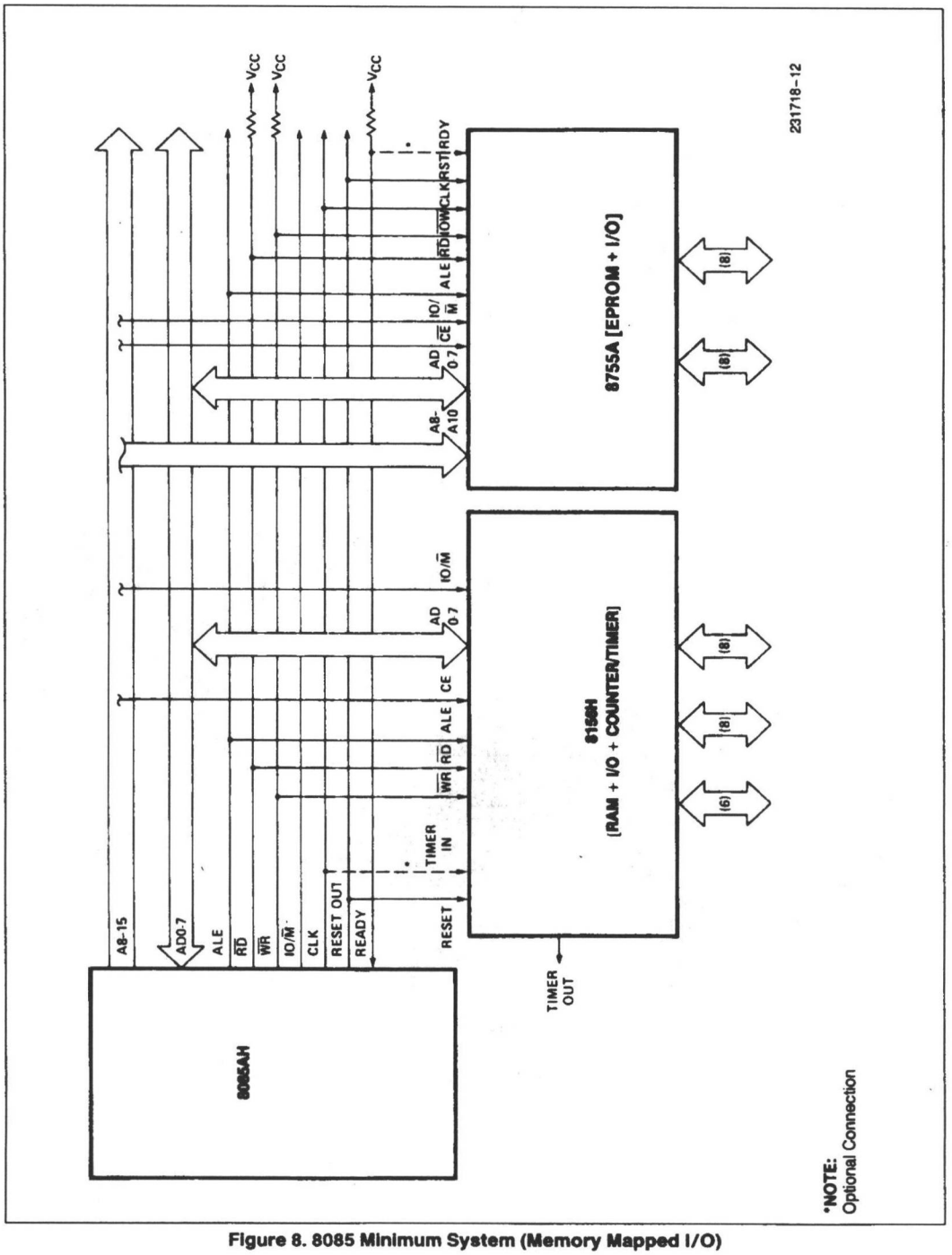


Figure 8. 8085 Minimum System (Memory Mapped I/O)

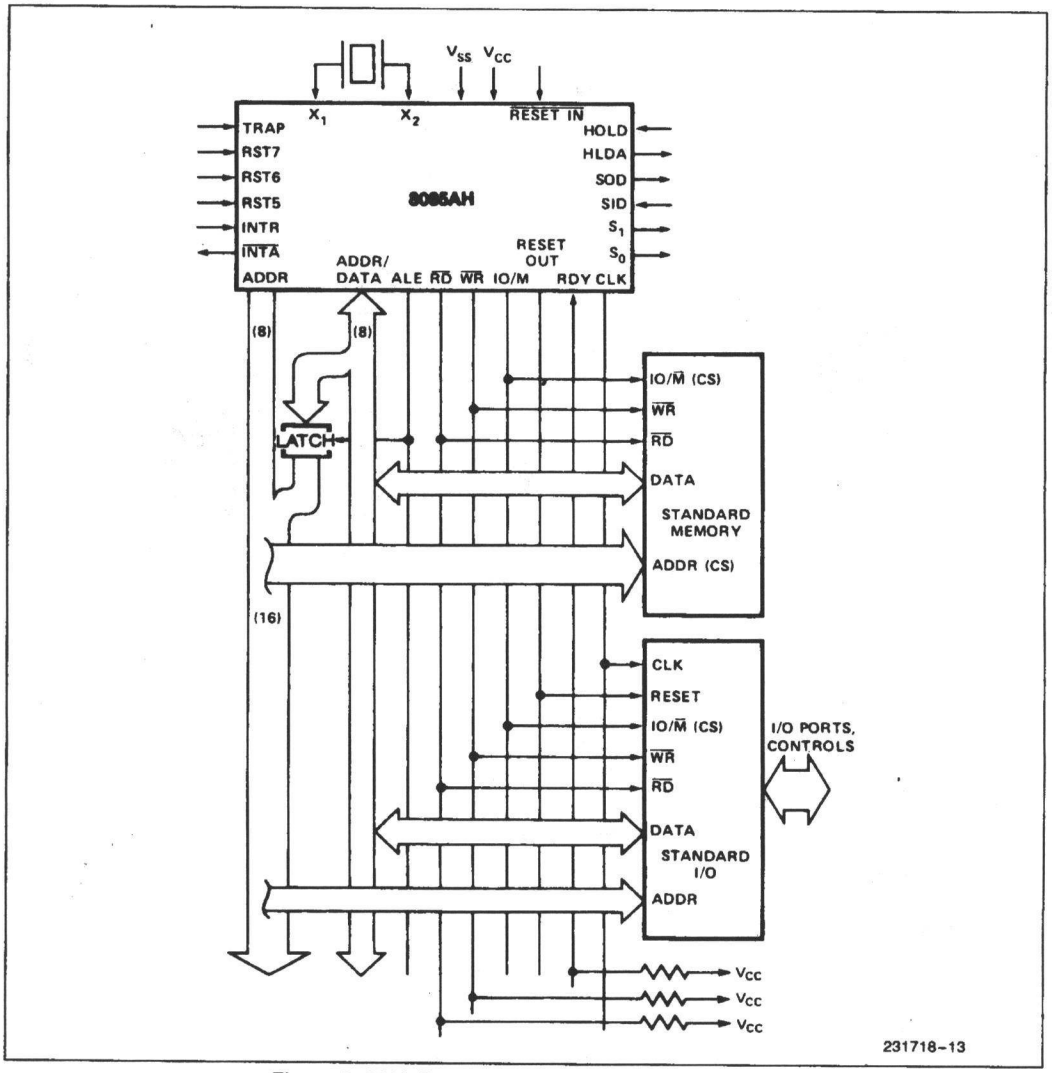


Figure 9. 8085 System (Using Standard Memories)

BASIC SYSTEM TIMING

The 8085AH has a multiplexed Data Bus. ALE is used as a strobe to sample the lower 8-bits of address on the Data Bus. Figure 10 shows an instruction fetch, memory read and I/O write cycle (as would occur during processing of the OUT instruction). Note that during the I/O write and read cycle that the I/O port address is copied on both the upper and lower half of the address.

There are seven possible types of machine cycles. Which of these seven takes place is defined by the status of the three status lines ($IO/\overline{M}$, S_1, S_0) and the three control signals ($\overline{RD}$, $\overline{WR}$, and $\overline{INTA}$). (See Table 3.) The status lines can be used as advanced controls (for device selection, for example), since they become active at the T_1 state, at the outset of each machine cycle. Control lines $\overline{RD}$ and $\overline{WR}$ become active later, at the time when the transfer of data is to take place, so are used as command lines.

A machine cycle normally consists of three T states, with the exception of OPCODE FETCH, which normally has either four or six T states (unless $\overline{WAIT}$ or HOLD states are forced by the receipt of $\overline{READY}$ or HOLD inputs). Any T state must be one of ten possible states, shown in Table 4.

Table 3. 8085AH Machine Cycle Chart

Machine Cycle			Status			Control		
			$IO/\overline{M}$	S1	S0	$\overline{RD}$	$\overline{WR}$	$\overline{INTA}$
OPCODE FETCH	(OF)		0	1	1	0	1	1
MEMORY READ	(MR)		0	1	0	0	1	1
MEMORY WRITE	(MW)		0	0	1	1	0	1
I/O READ	(IOR)		1	1	0	0	1	1
I/O WRITE	(IOW)		1	0	1	1	0	1
ACKNOWLEDGE OF INTR	(INA)		1	1	1	1	1	0
BUS IDLE	(BI):	DAD	0	1	0	1	1	1
		ACK.OF RST,TRAP	1	1	1	1	1	1
		HALT	TS	0	0	TS	TS	1

Table 4. 8085AH Machine State Chart

Machine State	Status & Buses				Control		
	S1,S0	$IO/\overline{M}$	A_8–A_{15}	AD_0–AD_7	$\overline{RD}$, $\overline{WR}$	$\overline{INTA}$	ALE
T_1	X	X	X	X	1	1	1*
T_2	X	X	X	X	X	X	0
T_{WAIT}	X	X	X	X	X	X	0
T_3	X	X	X	X	X	X	0
T_4	1	0†	X	TS	1	1	0
T_5	1	0†	X	TS	1	1	0
T_6	1	0†	X	TS	1	1	0
T_{RESET}	X	TS	TS	TS	TS	1	0
T_{HALT}	0	TS	TS	TS	TS	1	0
T_{HOLD}	X	TS	TS	TS	TS	1	0

0 = Logic "0" TS = High Impedance
1 = Logic "1" X = Unspecified
*ALE not generated during 2nd and 3rd machine cycles of DAD instruction.
†$IO/\overline{M}$ = 1 during T_4–T_6 of INA machine cycle.

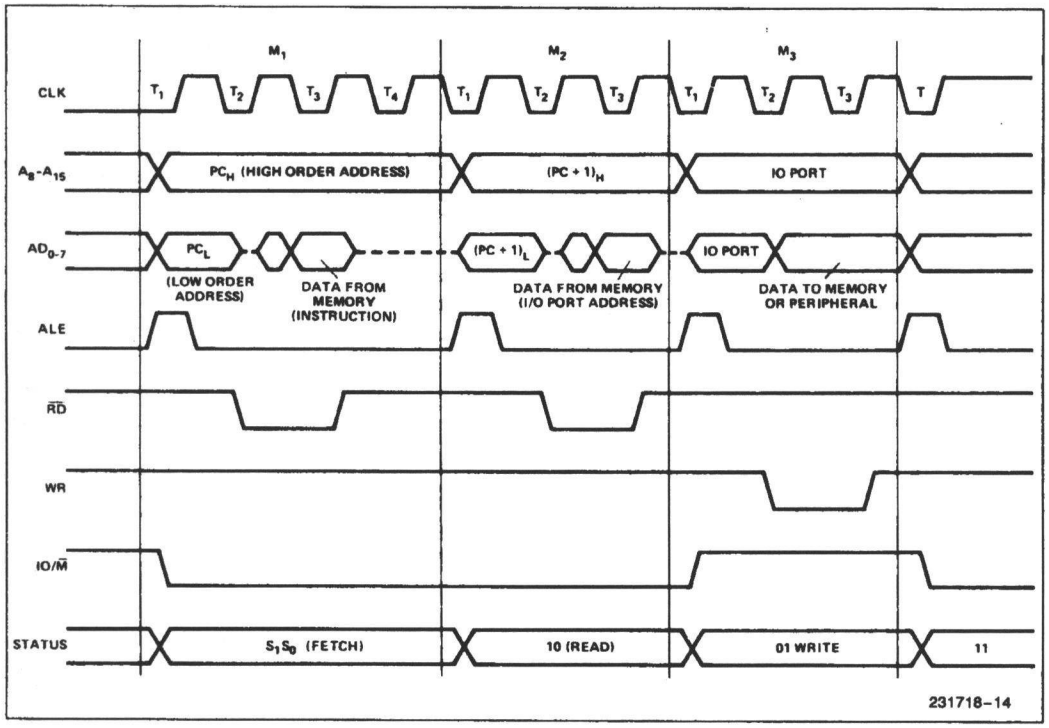


Figure 10. 8085AH Basic System Timing

ABSOLUTE MAXIMUM RATINGS*

Ambient Temperature under Bias .....0°C to 70°C
Storage Temperature .....−65°C to +150°C
Voltage on Any Pin with Respect to Ground.....−0.5V to +7V
Power Dissipation.....1.5W

NOTICE: This is a production data sheet. The specifications are subject to change without notice.

**WARNING: Stressing the device beyond the "Absolute Maximum Ratings" may cause permanent damage. These are stress ratings only. Operation beyond the "Operating Conditions" is not recommended and extended exposure beyond the "Operating Conditions" may affect device reliability.*

D.C. CHARACTERISTICS

8085AH, 8085AH-2: T_A = 0°C to 70°C, V_{CC} = 5V ±10%, V_{SS} = 0V; unless otherwise specified*
8085AH-1: T_A = 0°C to 70°C, V_{CC} = 5V ±5%, V_{SS} = 0V; unless otherwise specified*

Symbol	Parameter	Min	Max	Units	Test Conditions
V_{IL}	Input Low Voltage	−0.5	+0.8	V	
V_{IH}	Input High Voltage	2.0	V_{CC} +0.5	V	
V_{OL}	Output Low Voltage		0.45	V	I_{OL} = 2 mA
V_{OH}	Output High Voltage	2.4		V	I_{OH} = −400 μA
I_{CC}	Power Supply Current		135	mA	8085AH, 8085AH-2
			200	mA	8085AH-1
I_{IL}	Input Leakage		±10	μA	$0 \le V_{IN} \le V_{CC}$
I_{LO}	Output Leakage		±10	μA	$0.45V \le V_{OUT} \le V_{CC}$
V_{ILR}	Input Low Level, RESET	−0.5	+0.8	V	
V_{IHR}	Input High Level, RESET	2.4	V_{CC} + 0.5	V	
V_{HY}	Hysteresis, RESET	0.15		V	

A.C. CHARACTERISTICS

8085AH, 8085AH-2: T_A = 0°C to 70°C, V_{CC} = 5V ±10%, V_{SS} = 0V*
8085AH-1: T_A = 0°C to 70°C, V_{CC} = 5V ±5%, V_{SS} = 0V

Symbol	Parameter	8085AH (2)		8085AH-2 (2)		8085AH-1 (2)		Units
		Min	Max	Min	Max	Min	Max	
t_{CYC}	CLK Cycle Period	320	2000	200	2000	167	2000	ns
t_1	CLK Low Time (Standard CLK Loading)	80		40		20		ns
t_2	CLK High Time (Standard CLK Loading)	120		70		50		ns
t_r, t_f	CLK Rise and Fall Time		30		30		30	ns
t_{XKR}	X_1 Rising to CLK Rising	20	120	20	100	20	100	ns
t_{XKF}	X_1 Rising to CLK Falling	20	150	20	110	20	110	ns
t_{AC}	A_{8-15} Valid to Leading Edge of Control (1)	270		115		70		ns
t_{ACL}	A_{0-7} Valid to Leading Edge of Control	240		115		60		ns
t_{AD}	A_{0-15} Valid to Valid Data In		575		350		225	ns
t_{AFR}	Address Float after Leading Edge of $\overline{READ}$ ($\overline{INTA}$)		0		0		0	ns
t_{AL}	A_{8-15} Valid before Trailing Edge of ALE (1)	115		50		25		ns

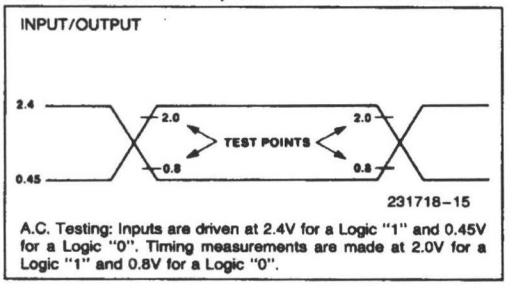
NOTE:
For Extended Temperature EXPRESS use M8085AH Electricals Parameters.

A.C. CHARACTERISTICS (Continued)

Symbol	Parameter	8085AH (2)		8085AH-2 (2)		8085AH-1 (2)		Units
		Min	Max	Min	Max	Min	Max	
t_{ALL}	A_{0-7} Valid before Trailing Edge of ALE	90		50		25		ns
t_{ARY}	READY Valid from Address Valid		220		100		40	ns
t_{CA}	Address (A_{8-15}) Valid after Control	120		60		30		ns
t_{CC}	Width of Control Low ($\overline{RD}$, $\overline{WR}$, $\overline{INTA}$) Edge of ALE	400		230		150		ns
t_{CL}	Trailing Edge of Control to Leading Edge of ALE	50		25		0		ns
t_{DW}	Data Valid to Trialing Edge of $\overline{WRITE}$	420		230		140		ns
t_{HABE}	HLDA to Bus Enable		210		150		150	ns
t_{HABF}	Bus Float after HLDA		210		150		150	ns
t_{HACK}	HLDA Valid to Trailing Edge of CLK	110		40		0		ns
t_{HDH}	HOLD Hold Time	0		0		0		ns
t_{HDS}	HOLD Setup Time to Trailing Edge of CLK	170		120		120		ns
t_{INH}	INTR Hold Time	0		0		0		ns
t_{INS}	INTR, RST, and TRAP Setup Time to Falling Edge of CLK	160		150		150		ns
t_{LA}	Address Hold Time after ALE	100		50		20		ns
t_{LC}	Trailing Edge of ALE to Leading Edge of Control	130		60		25		ns
t_{LCK}	ALE Low During CLK High	100		50		15		ns
t_{LDR}	ALE to Valid Data during Read		460		270		175	ns
t_{LDW}	ALE to Valid Data during Write		200		140		110	ns
t_{LL}	ALE Width	140		80		50		ns
t_{LRY}	ALE to READY Stable		110		30		10	ns
t_{RAE}	Trailing Edge of $\overline{READ}$ to Re-Enabling of Address	150		90		50		ns
t_{RD}	$\overline{READ}$ (or $\overline{INTA}$) to Valid Data		300		150		75	ns
t_{RV}	Control Trailing Edge to Leading Edge of Next Control	400		220		160		ns
t_{RDH}	Data Hold Time after $\overline{READ}$ $\overline{INTA}$	0		0		0		ns
t_{RYH}	READY Hold Time	0		0		5		ns
t_{RYS}	READY Setup Time to Leading Edge of CLK	110		100		100		ns
t_{WD}	Data Valid after Trailing Edge of $\overline{WRITE}$	100		60		30		ns
t_{WDL}	LEADING Edge of $\overline{WRITE}$ to Data Valid		40		20		30	ns

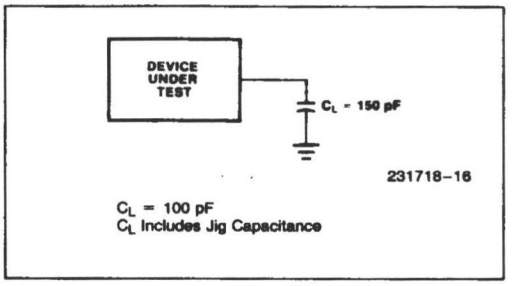
NOTES:
1. A_8–A_{15} address Specs apply IO/$\overline{M}$, S_0, and S_1 except A_8–A_{15} are undefined during T_4–T_6 of OF cycle whereas IO/$\overline{M}$, S_0, and S_1 are stable.
2. *Test Conditions:* t_{CYC} = 320 ns (8085AH)/200 ns (8085AH-2);/167 ns (8085AH-1); C_L = 150 pF.
3. For all output timing where C ≠ 150 pF use the following correction factors:
   25 pF ≤ C_L < 150 pF: −0.10 ns/pF
   150 pF < C_L ≤ 300 pF: +0.30 ns/pF
4. Output timings are measured with purely capacitive load.
5. To calculate timing specifications at other values of t_{CYC} use Table 5.

A.C. TESTING INPUT, OUTPUT WAVEFORM



A.C. Testing: Inputs are driven at 2.4V for a Logic "1" and 0.45V for a Logic "0". Timing measurements are made at 2.0V for a Logic "1" and 0.8V for a Logic "0".

A.C. TESTING LOAD CIRCUIT



C_L = 100 pF
C_L Includes Jig Capacitance

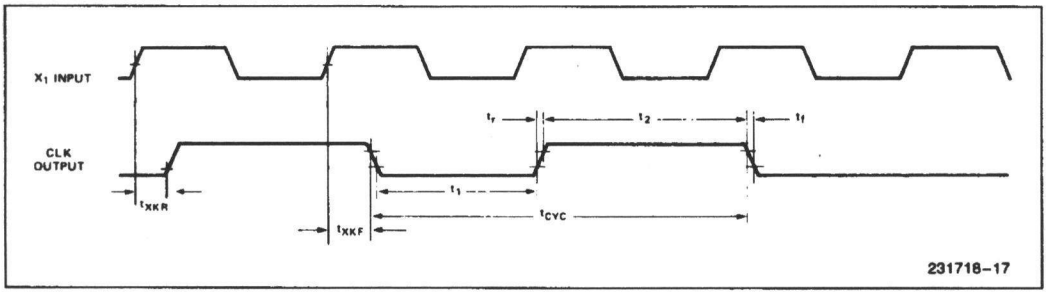
Table 5. Bus Timing Specification as a T_{CYC} Dependent

Symbol	8085AH	8085AH-2	8085AH-1	
t_{AL}	(1/2)T − 45	(1/2)T − 50	(1/2)T − 58	Minimum
t_{LA}	(1/2)T − 60	(1/2)T − 50	(1/2)T − 63	Minimum
t_{LL}	(1/2)T − 20	(1/2)T − 20	(1/2)T − 33	Minimum
t_{LCK}	(1/2)T − 60	(1/2)T − 50	(1/2)T − 68	Minimum
t_{LC}	(1/2)T − 30	(1/2)T − 40	(1/2)T − 58	Minimum
t_{AD}	(5/2 + N)T − 225	(5/2 + N)T − 150	(5/2 + N)T − 192	Maximum
t_{RD}	(3/2 + N)T − 180	(3/2 + N)T − 150	(3/2 + N)T − 175	Maximum
t_{RAE}	(1/2)T − 10	(1/2)T − 10	(1/2)T − 33	Minimum
t_{CA}	(1/2)T − 40	(1/2)T − 40	(1/2)T − 53	Minimum
t_{DW}	(3/2 + N)T − 60	(3/2 + N)T − 70	(3/2 + N)T − 110	Minimum
t_{WD}	(1/2)T − 60	(1/2)T − 40	(1/2)T − 53	Minimum
t_{CC}	(3/2 + N)T − 80	(3/2 + N)T − 70	(3/2 + N)T − 100	Minimum
t_{CL}	(1/2)T − 110	(1/2)T − 75	(1/2)T − 83	Minimum
t_{ARY}	(3/2)T − 260	(3/2)T − 200	(3/2)T − 210	Maximum
t_{HACK}	(1/2)T − 50	(1/2)T − 60	(1/2)T − 83	Minimum
t_{HABF}	(1/2)T + 50	(1/2)T + 50	(1/2)T + 67	Maximum
t_{HABE}	(1/2)T + 50	(1/2)T + 50	(1/2)T + 67	Maximum
t_{AC}	(2/2)T − 50	(2/2)T − 85	(2/2)T − 97	Minimum
t_1	(1/2)T − 80	(1/2)T − 60	(1/2)T − 63	Minimum
t_2	(1/2)T − 40	(1/2)T − 30	(1/2)T − 33	Minimum
t_{RV}	(3/2)T − 80	(3/2)T − 80	(3/2)T − 90	Minimum
t_{LDR}	(4/2 + N)T − 180	(4/2)T − 130	(4/2)T − 159	Maximum

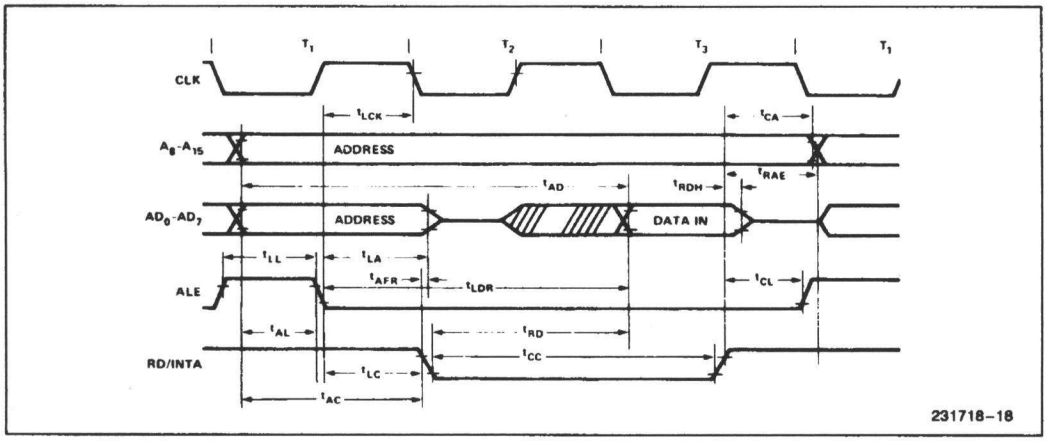
NOTE:
N is equal to the total WAIT states. T = t_{CYC}.

WAVEFORMS

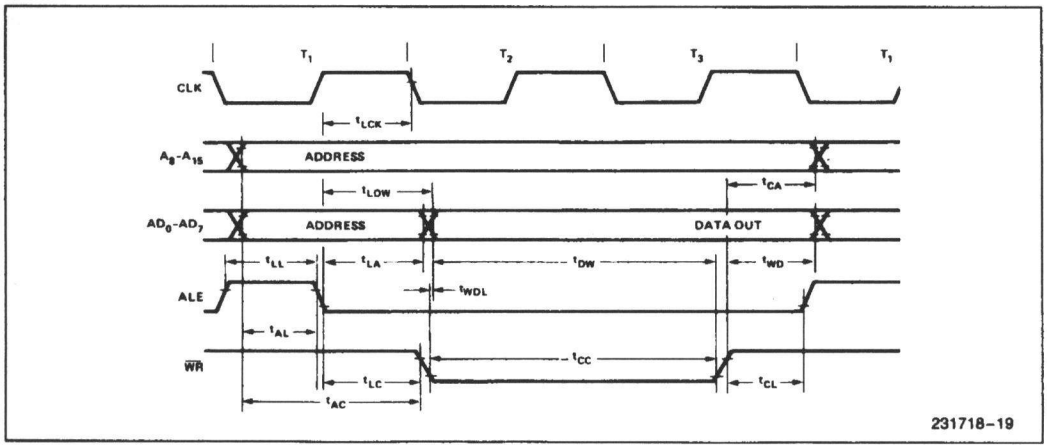
CLOCK



READ

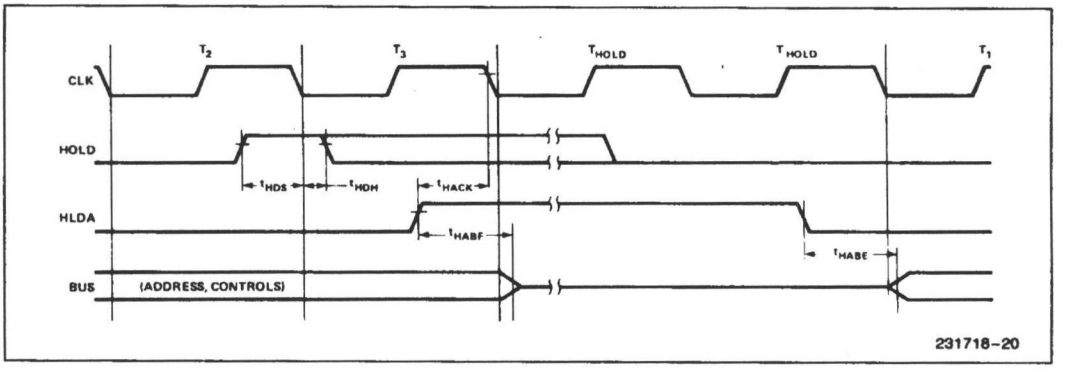


WRITE

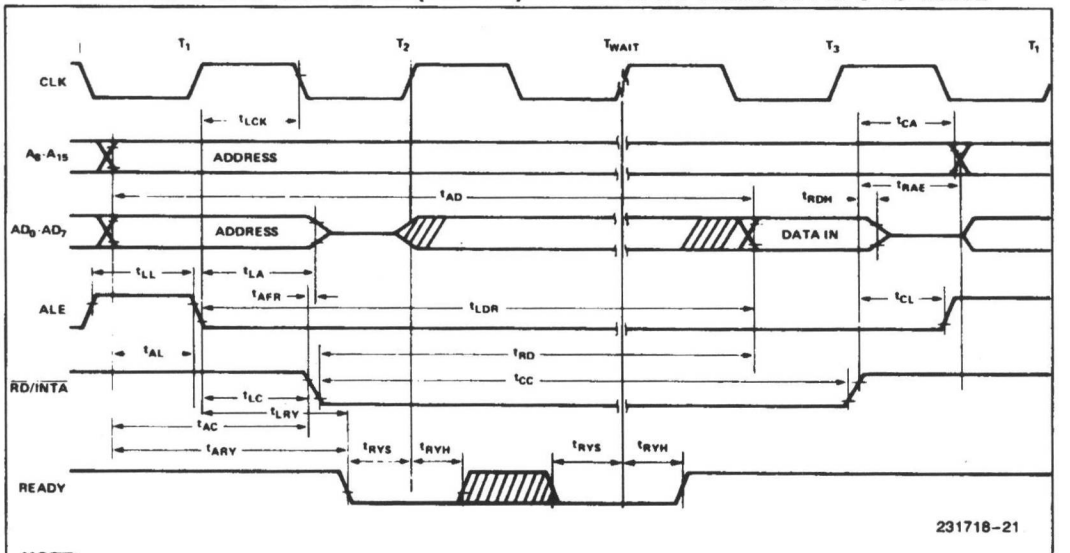


WAVEFORMS (Continued)

HOLD



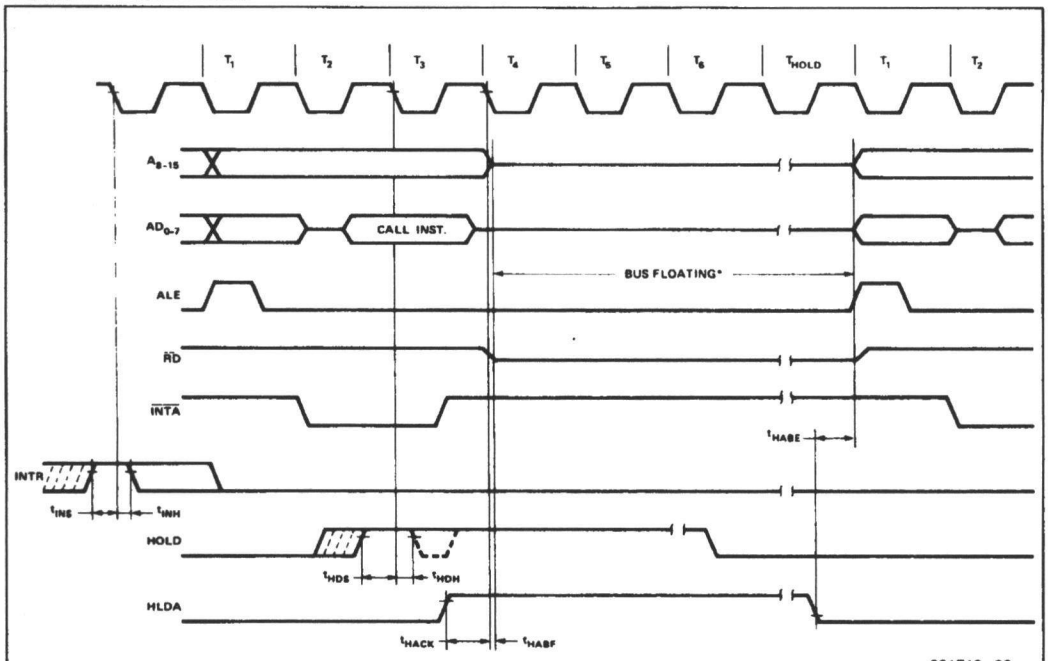
READ OPERATION WITH WAIT CYCLE (TYPICAL)—SAME READY TIMING APPLIES TO WRITE



NOTE:
1. Ready must remain stable during setup and hold times.

WAVEFORMS (Continued)

INTERRUPT AND HOLD



*NOTE:
IO/M is also floating during this time.

Table 6. Instruction Set Summary

Mnemonic	Instruction Code D_7 D_6 D_5 D_4 D_3 D_2 D_1 D_0								Operations Description
MOVE, LOAD AND STORE									
MOVr1 r2	0	1	D	D	D	S	S	S	Move register to register
MOV M.r	0	1	1	1	0	S	S	S	Move register to memory
MOV r.M	0	1	D	D	D	1	1	0	Move memory to register
MVI r	0	0	D	D	D	1	1	0	Move immediate register
MVI M	0	0	1	1	0	1	1	0	Move immediate memory
LXI B	0	0	0	0	0	0	0	1	Load immediate register Pair B & C
LXI D	0	0	0	1	0	0	0	1	Load immediate register Pair D & E
LXI H	0	0	1	0	0	0	0	1	Load immediate register Pair H & L
STAX B	0	0	0	0	0	0	1	0	Store A indirect
STAX D	0	0	0	1	0	0	1	0	Store A indirect
LDAX B	0	0	1	0	1	0	1	0	Load A indirect
LDAX D	0	0	0	1	1	0	1	0	Load A indirect
STA	0	0	1	1	0	0	1	0	Store A direct
LDA	0	0	1	1	1	0	1	0	Load A direct
SHLD	0	0	1	0	0	0	1	0	Store H & L direct
LHLD	0	0	1	0	1	0	1	0	Load H & L direct
XCHG	1	1	1	0	1	0	1	1	Exchange D & E, H & L Registers
STACK OPS									
PUSH B	1	1	0	0	0	1	0	1	Push register Pair B & C on stack
PUSH D	1	1	0	1	0	1	0	1	Push register Pair D & E on stack
PUSH H	1	1	1	0	0	1	0	1	Push register Pair H & L on stack
PUSH PSW	1	1	1	1	0	1	0	1	Push A and Flags on stack
POP B	1	1	0	0	0	0	0	1	Pop register Pair B & C off stack
POP D	1	1	0	1	0	0	0	1	Pop register Pair D & E off stack
POP H	1	1	1	0	0	0	0	1	Pop register Pair H & L off stack

Mnemonic	Instruction Code D_7 D_6 D_5 D_4 D_3 D_2 D_1 D_0								Operations Description
STACK OPS (Continued)									
POP PSW	1	1	1	1	0	0	0	1	Pop A and Flags off stack
XTHL	1	1	1	0	0	0	1	1	Exchange top of stack, H & L
SPHL	1	1	1	1	1	0	0	1	H & L to stack pointer
LXI SP	0	0	1	1	0	0	0	1	Load immediate stack pointer
INX SP	0	0	1	1	0	0	1	1	Increment stack pointer
DCX SP	0	0	1	1	1	0	1	1	Decrement stack pointer
JUMP									
JMP	1	1	0	0	0	0	1	1	Jump unconditional
JC	1	1	0	1	1	0	1	0	Jump on carry
JNC	1	1	0	1	0	0	1	0	Jump on no carry
JZ	1	1	0	0	1	0	1	0	Jump on zero
JNZ	1	1	0	0	0	0	1	0	Jump on no zero
JP	1	1	1	1	0	0	1	0	Jump on positive
JM	1	1	1	1	1	0	1	0	Jump on minus
JPE	1	1	1	0	1	0	1	0	Jump on parity even
JPO	1	1	1	0	0	0	1	0	Jump on parity odd
PCHL	1	1	1	0	1	0	0	1	H & L to program counter
CALL									
CALL	1	1	0	0	1	1	0	1	Call unconditional
CC	1	1	0	1	1	1	0	0	Call on carry
CNC	1	1	0	1	0	1	0	0	Call on no carry
CZ	1	1	0	0	1	1	0	0	Call on zero
CNZ	1	1	0	0	0	1	0	0	Call on no zero
CP	1	1	1	1	0	1	0	0	Call on positive
CM	1	1	1	1	1	1	0	0	Call on minus
CPE	1	1	1	0	1	1	0	0	Call on parity even
CPO	1	1	1	0	0	1	0	0	Call on parity odd
RETURN									
RET	1	1	0	0	1	0	0	1	Return
RC	1	1	0	1	1	0	0	0	Return on carry
RNC	1	1	0	1	0	0	0	0	Return on no carry
RZ	1	1	0	0	1	0	0	0	Return on zero